MAY 2011

D-TA SYSTEMS INC.

Sensor Processing for Demanding Applications




RADIO • RADAR • SONAR • ACOUSTICS • TEST & MEASUREMENT

Our Mission

D-TA Systems was established in 2007 with the mandate to simplify the development of complex sonar, radar, communications, and test and measurement systems. Our goal is to cut the development time and cost. We have successfully addressed that mandate by using a multidisciplinary and highly talented team who share the goal of providing groundbreaking solutions to our customers. The D-TA management team has extensive experience in the development and deployment of complex sensor processing systems, including the world's first COTS sonar; the standardization of FPDP data flow architecture; and software radio design concepts. We draw on our impressive background and determined sense of innovation to provide our customers with a modern and pain-free approach to sensor processing.

D-TA Systems has moved away from offering board-level COTS products, as these types of products can take significant time to integrate and test, leaving customers with huge hidden costs. We offer an attractive alternative: reconfigurable box-level COTS products that offer virtually "plug and play" solutions.

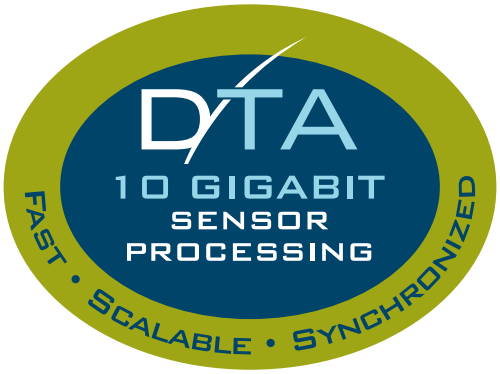
To address the high-bandwidth and high-channel-count requirements of today's demanding sensor processing problems, D-TA has pioneered 10 Gigabit Sensor Processing by leveraging the standard 10 Gigabit network technology. D-TA's 10 Gigabit Sensor Processing technology guarantees sustained data transfer at rates close to the line rate (1 GByte/s); virtually limitless scalability; and synchronization across multiple 10 Gigabit networks, without sacrificing analog performance.

To address the full range of customer demands, D-TA Systems has developed end-to-end solutions for rapid system integration. From RF to Network to Multi-Core Software processing, we are able to support you completely for rapid deployment of your concept.

10 Gigabit Sensor Processing

ULTRA-FAST, SCALABLE AND SYNCHRONIZED

D-TA Systems has pioneered 10 Gigabit Sensor Processing to handle the demanding requirements of today's high-bandwidth and high-channel-count systems. D-TA's 10 Gigabit Sensor Processing sustains data throughput rates close to the line rate with no loss of data samples. D-TA's design also ensures virtually limitless scalability and fully synchronous operation. A demonstration of this is D-TA's Record & Playback product, which sustains record/playback rates over 3.2 GBytes/s using four networks. Furthermore, D-TA's 10 Gigabit Sensor processing is OS agnostic, facilitating greater software portability. The use of optical fibers allows separation of signal digitization and processing functions over long distances, permitting digitization close to the sensors. D-TA has also successfully developed a Software Development Framework for real-time processing using Multi-Core servers.



[Download Tech Notes TN-1, TN-2 and TN-3 for more information on D-TA's product philosophy and products and Tech Note TN-15 on the advantages of 10 Gigabit Sensor Processing]

Content

DTA-3290

20 MHz - 6GHz TURNABLE SOFTWARE RADIO TRANSCEIVER

DTA-3290 is a complete Software Defined Radio (SDR) with a flexible RF front end. Like all D-TA products, the DTA-3290 includes a 10 Gigabit network for easy connectivity to a server for real-time post-processing. Designed for processing a 40 MHz instantaneous bandwidth, it consists of two major components. The first is a single channel (antenna) RF section with a tunable Up Converter (UCON) and a Down Converter (DCON). The second is a Digital IF section with a 16-bit ADC, 16-bit Dual DACs, a large Virtex 5 FPGA, a 10 GbE network for high-speed data transfer, and a 1 GbE link for control. The Xilinx SX95T FPGA comes pre-configured with a DDC core that supports programmable decimation (from 2 to 32) for various bandwidth selections. The data at the output of the DDC is complex (I & Q). The Digital Up Conversion (DUC) is built in the Dual DAC chip and supports interpolation of 2, 4 or 8 for up-sampling prior to up-conversion by a programmable NCO. Only the real part of the complex DAC outputs is used for RF up-conversion. To support customer development, D-TA offers an FPGA Development Kit (FDK) as well as software development support for Multi-Core servers.

[Download Tech Note TN-20 for detailed information on DTA-3290]

DTA-3290 (1U x 19" x 20")

AT A GLANCE

- 20 MHz to 6 GHz Frequency Coverage
- 40 MHz Instantaneous BW
- Separate UCON & DCON Synthesizers for Independen Receive & Transmit
- 16 bit 130 MSPS ADC
- 16-Bit 500 MSPS Dual DACs
- Programmable Xilinx Virtex-5 FPGA
- Standard Programmable DDC Core
- 10 Gigabit Network for Data
- 1 Gigabit Network for Control
- Optional 1 Gigabit Network for Data (Low BW Applications)
- Multiple DTA-3290 can be Synchronized
- Optional DTA-1000 Multi-Core Server With 10 Gigabit NIC & Up to 8 Terabyte Storage
- Software & Firmware Development Kit
- Software Options include: Spectral Monitoring, Signal Detection, Intelligent Recording, Automatic Modulation Recognition, Arbitrary Waveform Generation, Radar Processing, etc.

APPLICATIONS

- Spectral Monitoring
- COMINT / SIGINT
- Cognitive Radio
- Waveform Research
- RF Test & Simulation
- Mobile & Satellite Systems
- Radar
- Sonobuoy
- TDOA & DF Systems

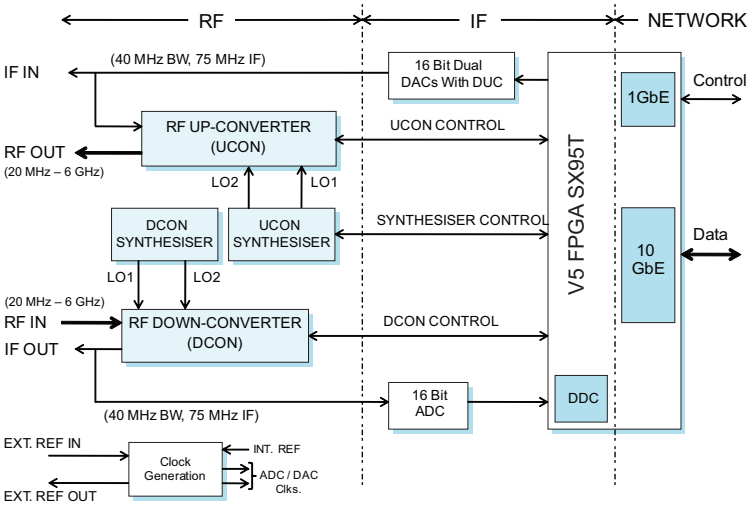
RF Section

The RF DCON uses a two-stage conversion process to produce a 75 MHz IF signal with a 40 MHz BW. The DCON features four pre-selector filters for better than 80 dB image rejection and three programmable attenuators for gain control. The RF band is divided into four bands with 40 MHz overlap (other than between band 1 and band 2) among them. These four bands include one direct path with no conversion. The DCON front end allows the user to switch between two antennas to cover the 20 MHz to 6 GHz frequency range. The user can also choose a high gain, low noise figure (high sensitivity) mode or a low gain, high IP3 (LNA bypassed) mode. Users can also use a customized pre-selector filter for further performance enhancements. The 75 MHz IF, with a 40 MHz BW, is ideal for undersampling by a 100 MHz sampling clock, as it provides a uniform guard band on both sides of the IF band. The digital IF section of the DTA-3290 incorporates a 100 MHz TCXO to provide a stable sampling clock.

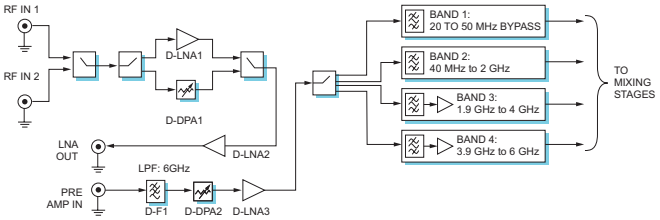
The Up Conversion (UCON) to RF also uses a two-stage conversion process. The first mixing stage converts the signal to a fixed internal IF. The second mixing stage converts the signal to the desired RF band. The band select filters, in turn, filter the other mixing products. There are eight RF paths, including one bypass path.

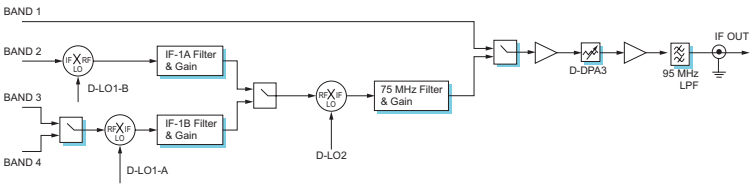
For dedicated HF processing, D-TA offers a DTA-3200H version to specifically handle the 2 MHz – 30 MHz HF band. The DTA-3290H version uses only the direct path, which requires no signal mixing. The filters are modified for the desired 3 MHz – 30 MHz band.

DTA-3290 Block Diagram

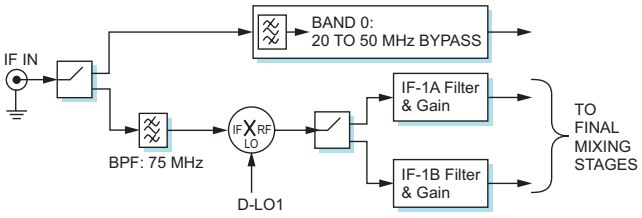


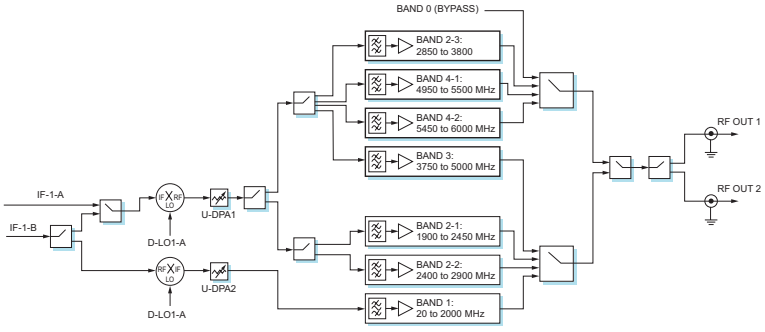
RF Down Conversion (DCON) Stage



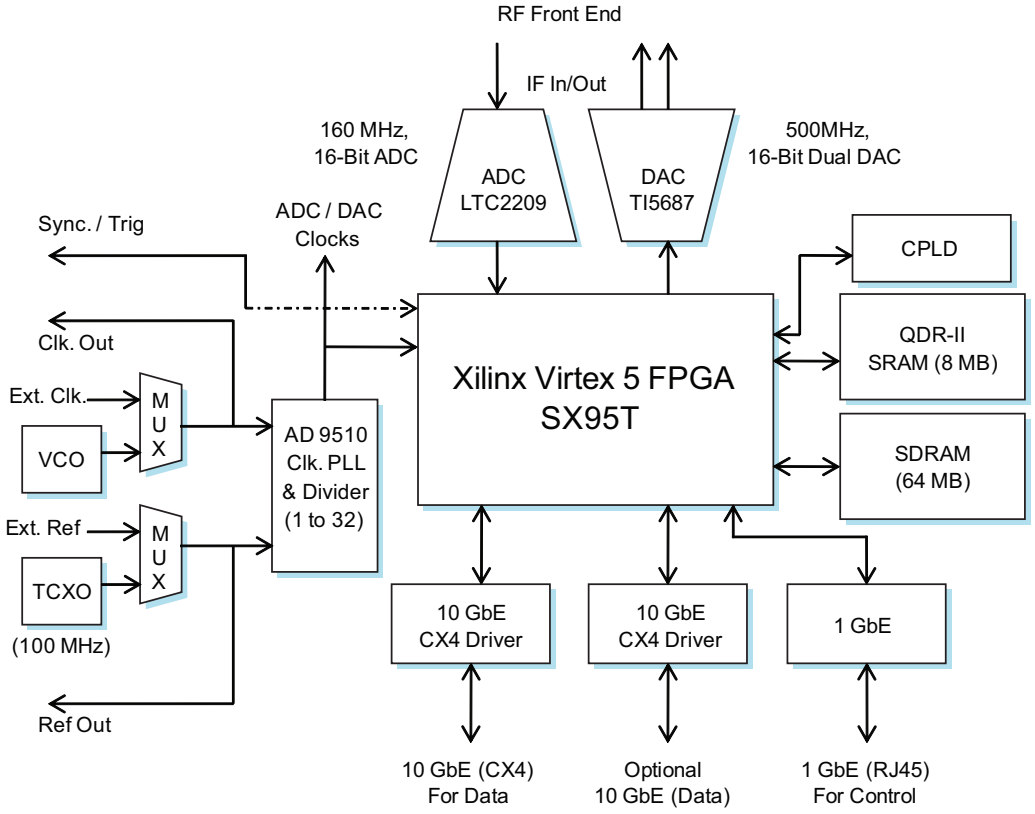


RF Up Conversion (UCON) Stage





Digital IF Section



The digital IF section includes 16-bit, 130 MHz ADC and 16-bit, 500 MHz interpolating dual DACs (for complex up-conversion to 75 MHz IF). Both ADC and DACs are connected to a large Virtex 5 FPGA (SX95T). The FPGA implements a DDC (Digital Down Converter for programmable bandwidth selection) with programmable decimations of 2, 4, 8, 16 and 32; and all 10 GbE (for data) and 1 GbE (for control) logic. The FPGA also acts as a controller for the UCON, DCON and RF Synthesizer modules.

The DAC includes programmable interpolation and up-conversion to provide complex IF signal. The RF UCON includes all necessary filtering to use only the real part of the DAC IF signal.

The DTA-3290 implements a very flexible clock generation scheme that allows the user to use the internal 100MHz TCXO to generate ADC, DAC clocks and reference signals for all LOs for the RF stages. An external reference can also be used to generate the clocks.

The Clk Out and Sync/Trig Out signals allow multiple DTA-3290 systems to be used in a synchronous fashion for phase-coherent applications.

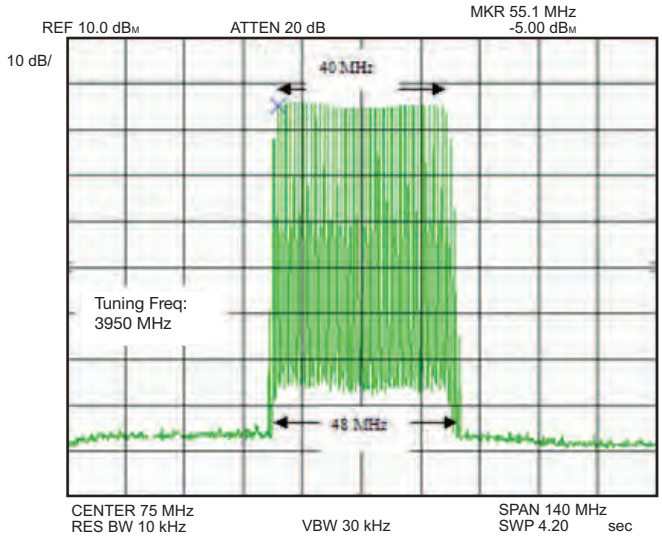
The digital IF section is also offered as a stand-alone product, called DTA-2210.

SPECIFICATIONS

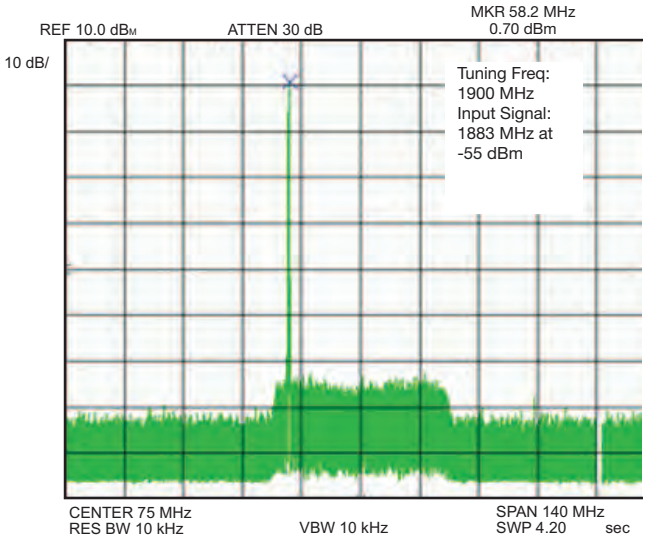
SPECIFICATIONS – RF	RECEIVER	TRANSMITTER	SPECIFICATIONS – IF	RECEIVER	TRANSMITTER
Frequency Range	20 MHz – 6 GHz	20 MHz – 6 GHz	No. of Data Converters	1 ADC	1 Complex DAC
Instantaneous BW	40 MHz	40 MHz	Precision	16 Bits	16 Bits
Tuning Resolution	200 kHz	200 kHz	DDC Decimation/ DUC Interpolation	2, 4, 8, 16 or 32 (FPGA based)	2, 4 or 8 (integrated with DACs)
Tuning Speed (contact factory for faster option)	<1 ms	<1 ms	SFDR (typical)	< 90 dBFS	< 70 dBFS
Gain	50 dB	0 dB	**SPECIFICATIONS – GENERAL**	**SYSTEM**	**COMMENTS**
Gain Control	62 dB in 1dB Steps	62 dB in 1dB Steps	Control	1 GbE	Copper RJ-45
Noise Figure	<8 dB		Data	10 GbE	Copper over CX4
OIP3	+30 dBm		Reference Clock	Internal or External	100 MHz (internal) 10MHz – 100 MHz (external)
Image Reject	80 dB	60 dB	Multi-Unit Synchronization	Yes	Sync., Trig., PPS and Ref. Signal are also offered as Outputs
Spurious	-70 dBc	-60 dBc	Operating Temp	0 to 50° C	
Output Power	0 dBm @IF	0 dBm @RF	Power	<125 W	110V or 220V
Synthesizer Phase Noise					
(See Tech Note 20 for details)	-94 dBc/Hz @100 kHz	-94 dBc/Hz @100 kHz	Dimensions and Weight	1U X 19" X 20", 20 lbs	

[Specifications may change without notice]

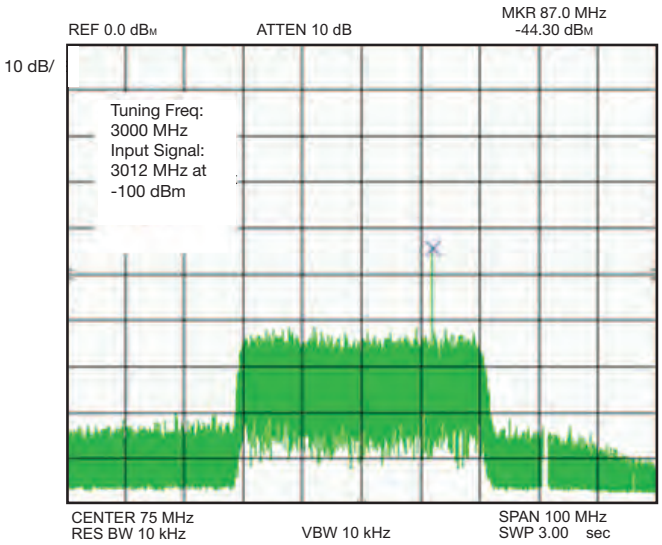
PERFORMANCE PLOTS



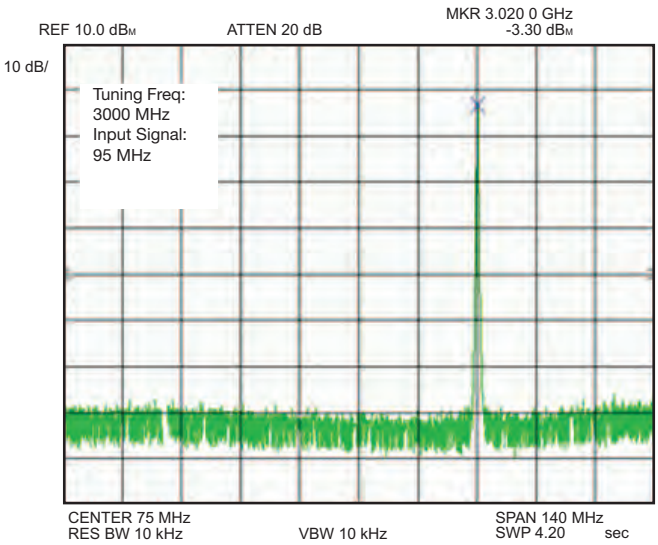
DCON Passband Response



DCON Response with 55dB Gain (-55 dBm Signal Input @ 1883 MHz)

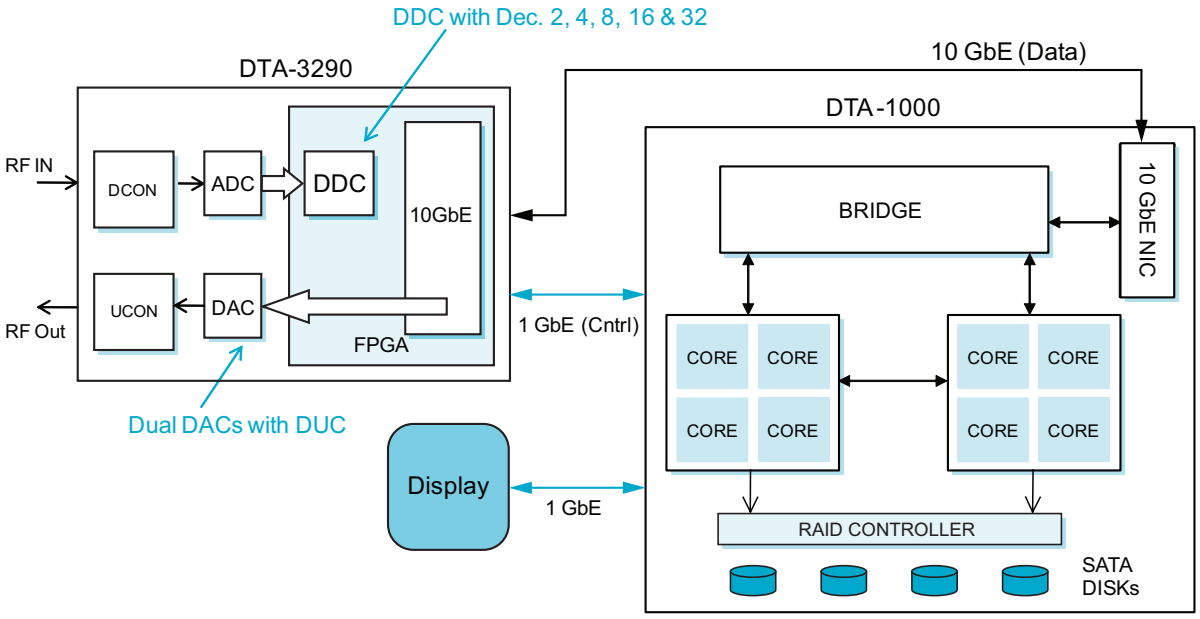


DCON Response with 55dB Gain (-100 dBm Signal Input @ 3012 MHz)



UCON Performance with 95 MHz Input (IF=75 MHz)

POST-PROCESSING



DTA-3290 provides a 10 Gigabit network that will connect to any server-class computer via a 10 Gigabit Network Interface Card (NIC). The 10 GbE interface is capable of supporting data transfer rates in excess of 800 MBytes/s on a sustained basis. To facilitate user application development, D-TA offers the DTA-1000 Multi-Core server (two quad core processors) that is integrated with the 10 GbE NIC and is installed with all necessary system software, including the D-TA Software Development Kit (SDK) for implementing real-time applications. The DTA-1000 is optionally available with up to 8 TB of storage for recording a full-bandwidth (40 MHz) signal to disk. Pre-recorded signals or computer-generated signals can also be played back in real time through the DTA-3290 transmitter.

D-TA Systems offers training for Multi-Core software development to speed up application development. Furthermore, a number of ready-to-run software application modules for DTA-1000 can be purchased. These include Spectral Monitoring & Signal Detection, Intelligent Recording, Automatic Modulation Recognition, and Arbitrary Waveform Generation. Interested parties should contact D-TA Systems for details.

OPTIONAL DATA TRANSFER OVER 1 GbE INTERFACE

For some applications involving narrowband signals (e.g., COMINT, SIGINT, communications, etc.), the data rate is so low that a 1 GbE link is adequate. This can be accomplished by removing the 10 GbE logic and implementing data transfer over the 1 GbE interface. D-TA products have the capability to implement additional 1 GbE link so that users can separate the data and control links over separate 1 GbE link for easy system architecting.

DTA-2210

DTA-2210 is a compact (1U X 19" X 10.5") Digital IF Transceiver (DTA-3290 without the RF section). It is a highly cost-effective option for users who have their own RF front end.

[Download Tech Note TN-4 for more information on DTA-2210]

FPGA CORE DEVELOPMENT

The DTA-3290 FPGA is pre-loaded with a standard programmable DDC core for convenient IF signal down conversion to baseband. For user core development, an optional Firmware Development Kit (FDK) with full source code is also available. The FDK is delivered in the Xilinx ISE environment and allows users to modify and add VHDL-based DSP processing modules.

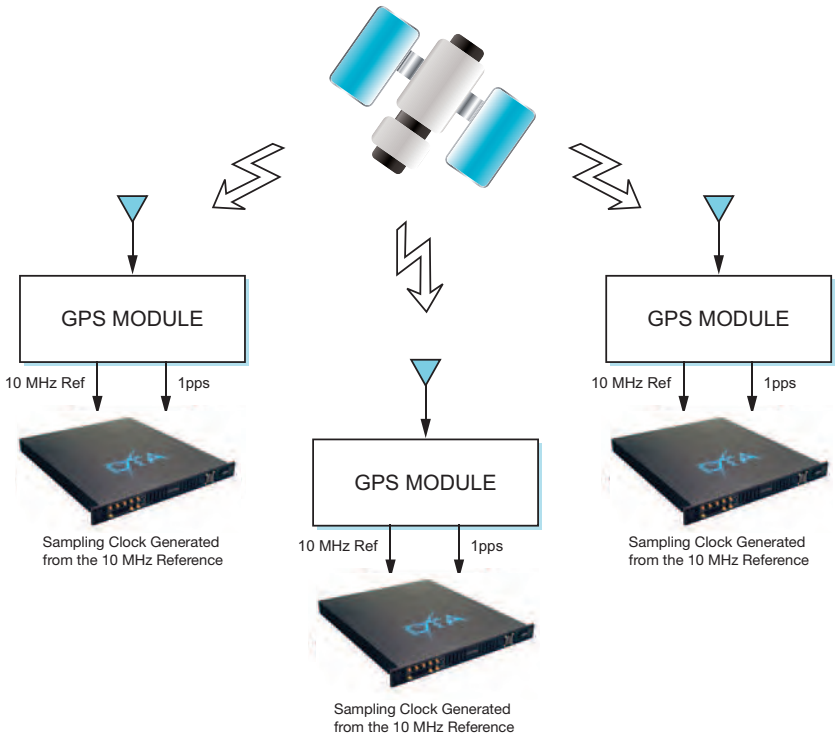
ORDERING INFORMATION

MODEL NO.	DESCRIPTION	REMARKS
DTA-3290W-1 R	Single Antenna 20MHz – 6GHz Software Radio (Rx. only)	
DTA-3290W-1 RT	Single Antenna 20MHz – 6GHz Software Radio Transceiver (Rx. & TX.)	
DTA-3290H-1 RT	Single Antenna 2 MHz – 30 MHz (HF) Software Radio Transceiver (Rx. & TX.)	
DTA-3290H-1 R	Single Antenna 2 MHz – 30 MHz (HF) Software Radio (Rx. only)	
DTA-2210-1 RT	Digital IF Transceiver (DTA-3290 without the RF section)	
SDK-3290	Full Source Software Development Kit for DTA-3290	
FDK-3290	Firmware Development Kit for DTA-3290	
DTA-1000 -R	2 X Quad Core Linux Server (1U) with NIC and SDK Pre-installed and 8 Terabytes of Disk Storage	Also available without the storage option
Application Software Modules	Spectral Monitoring & Signal Detection, Intelligent Recording, Automatic Modulation Recognition, Arbitrary Waveform Generation, etc.	Contact factory

DEPLOYING DTA-3290 FOR CHALLENGING APPLICATIONS

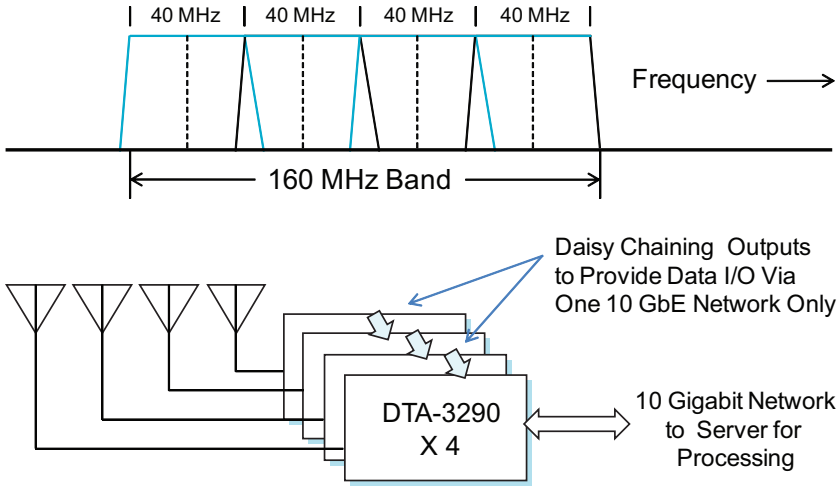
TDOA GEOLOCATION

Multiple DTA-3290 can be operated synchronously using GPS receivers. For estimation of the location of an unknown emission, the DTA-3290 outputs are transmitted (by fiber or wireless) to a central processing unit.



WIDEBAND SEARCH

Multiple DTA-3290 system can be used in parallel to search a large-frequency band to detect fast-frequency hopping signals or speed up the scan rate. Each 40 MHz band, digitized to 16 bits, also incorporates a large FPGA for fast FFT and/or other processing.



[Download Tech Note TN-09 for information on how to build Multi-Channel (Sonobuoy) Receivers]

DTA-3200

20 MHz – 6 GHz TUNABLE MULTI-ANTENNA SYNCHRONIZED RF TRANSCEIVER

DTA-3200 is a synchronized and tunable multi-channel RF up and down converter with frequency coverage up to 6 GHz. The DTA-3200 is designed for phase synchronous multi-channel operation with local oscillators in the conversion path being generated from the same synthesizer module. This makes it the ideal RF front end for applications like phase array radar, MIMO and direction finding. The DTA-3200 has a modular design that includes RF up converters (UCON), RF down converters (DCON), Synthesizer modules (one for UCON and one for DCON), and a digital controller. The RF UCON accepts a 75 MHz IF signal and converts it to the programmed RF frequency (up to 6 GHz), while the RF DCON down-converts an RF signal (up to 6 GHz) to a 75 MHz IF. The instantaneous bandwidth for the UCON and the DCON is 40 MHz. The DTA-3200 can be directly connected to the 16-channel IF transceiver unit, DTA-2300, for IF processing. The DTA-3200 is conveniently controlled over a 1 GbE link connected to the host computer. The controller also has a Virtex 5 FPGA that can be customized for advanced control options. A full source code SDK is available to control the DTA-3200 from an external host.

[Download Tech Notes TN-16 and TN-24 for detailed information on DTA-3200]

AT A GLANCE

- 20 MHz to 6 GHz frequency coverage
- 40 MHz Instantaneous BW @ 75 MHz IF (70 MHz optional)
- Designed for seamless operation with DTA-2300
- Up to 8 synchronized transceive channels in a single 3U high 19" rackmount enclosure
- Multiple DTA-3200s can be synchronized
- Separate UCON & DCON Synthesisers for independent Receive & Transmit
- All UCON/DCON channels are driven from common LO for phase coherence
- RF Switch matrix in UCON and DCON enables connection to band-specific antenna or PA
- Modular design allows optional configuration to have independent tuning across multiple channels
- Virtex-5 FPGA based controller allows custom scanning and fast control options
- 1 Gigabit Network for Control

APPLICATIONS

- Phased Array Radar
- Direction Finding
- COMINT / SIGINT
- MIMO
- Cognitive Radio
- Waveform Research
- RF Test & Simulation
- Mobile & Satellite Systems

DTA-3200 (3U X19" X20")

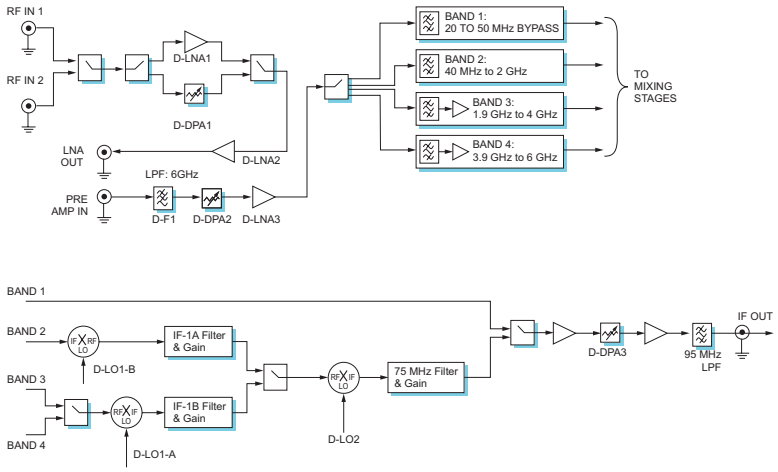
The DTA-3200 RF system is identical to the DTA-3290 RF front end, except that the DTA-3200 is designed for multi-antenna applications. The RF DCON uses a two-stage conversion process to produce a 75 MHz IF signal with a 40 MHz BW. The DCON features four pre-selector filters for better than 80 dB image rejection and three programmable attenuators for gain control. The RF band is divided into four bands with 40 MHz overlap (other than between band 1 and band 2) among them. These four bands include one direct path with no conversion. The DCON front end allows the user to switch between two antennas to cover the 20 MHz to 6 GHz frequency range. The user can also choose a high gain, low noise figure (high sensitivity) mode and/or a low gain, high IP3 (LNA bypassed) mode. Users can also use a customized pre-selector filter for further performance enhancements. The 75 MHz IF, with a 40 MHz BW, is ideal for under sampling by a 100 MHz sampling clock, as it provides a uniform guard band on both sides of the IF band. The DTA-2300 Digital IF Transceiver system incorporates a 100 MHz TCXO to provide a stable sampling clock.

The Up Conversion (UCON) to RF also uses a two-stage conversion process. The first mixing stage converts the signal to a fixed internal IF. The second mixing stage converts the signal to the desired RF band. The band select filters, in turn, filter the other mixing products. There are eight RF paths, including one bypass path.

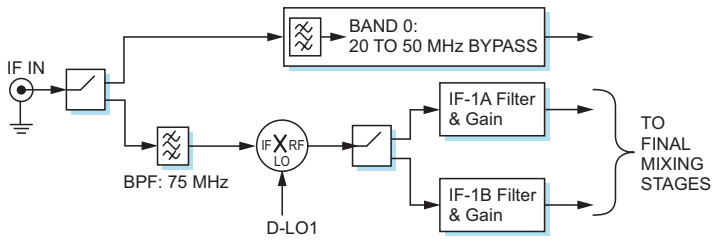
For all DCON modules, the two LO signals for mixing are generated by the same synthesizer. This is also true for all UCON modules.

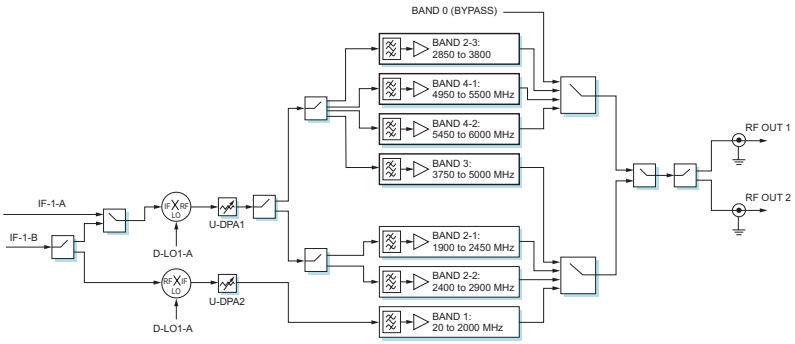
The DTA-3200 is also available for dedicated multi-antenna HF processing. The DTA-3200H version is configured to specifically handle the 2 MHz – 30 MHz HF band. The DTA-3290H uses only the direct path, which requires no signal mixing. The filters are modified for the desired 2 MHz – 30 MHz HF band.

RF Down Conversion (DCON) Stage



RF Up Conversion (UCON) Stage





SPECIFICATIONS

SPECIFICATIONS – RF	RECEIVER	TRANSMITTER	SPECIFICATIONS – RF	RECEIVER	TRANSMITTER
Frequency Range	20 MHz – 6 GHz	20 MHz – 6 GHz	Maximum Number of Channels in a 3U Enclosure	8 16 0	8 0 16
Instantaneous BW	40 MHz	40 MHz	Synthesizer Phase Noise	-94 dBc/Hz @100 kHz	-94 dBc/Hz @100 kHz
Tuning Resolution (smaller resolution possible)	200 kHz	200 kHz			
Tuning Speed (contact factory for faster option)	<1 ms	<1 ms	**SPECIFICATIONS – GENERAL**	**SYSTEM**	**COMMENTS**
Gain	50 dB	0 dB	Control	1 GbE	Copper RJ-45
Gain Control	62 dB in 1dB Steps	62 dB in 1dB Steps			
Noise Figure	<8 dB		Reference Clock	Internal or External	10 MHz or 100 MHz
OIP3	+30 dBm		Multi-Unit Synchronization	Yes	LOs are accessible from the outside
Image Reject	80 dB	60 dB	Operating Temp	0 to 50° C	
Spurious (typical)	-70 dBC	-60 dBC	Power	<400 W	8-ch UCON & DCON 110V or 220V
Maximum Output Power	0 dBm (IF)	0 dBm (RF)	Dimensions and Weight	3U X 19" X 20", 65 lbs	Fully populated

[Specifications may change without notice]

PERFORMANCE PLOTS

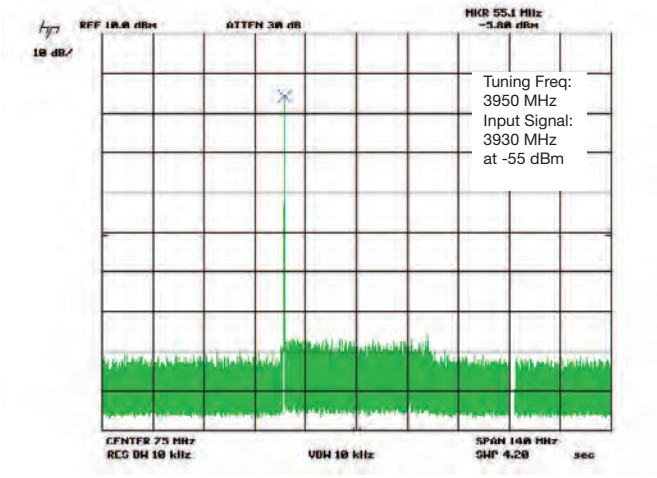


Figure 1: Down Converter tuned to 3950 MHz with 50 dB gain

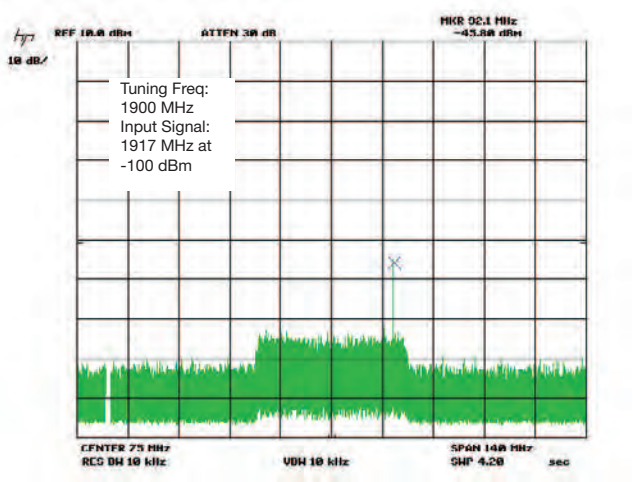


Figure 2: Down Converter tuned to 1900 MHz with 55 dB gain

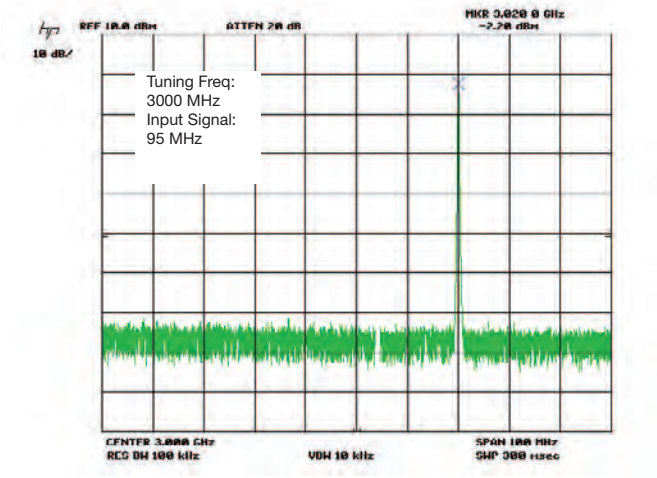


Figure 3: Up Converter Performance at 3000 MHz with 65 dB dynamic range

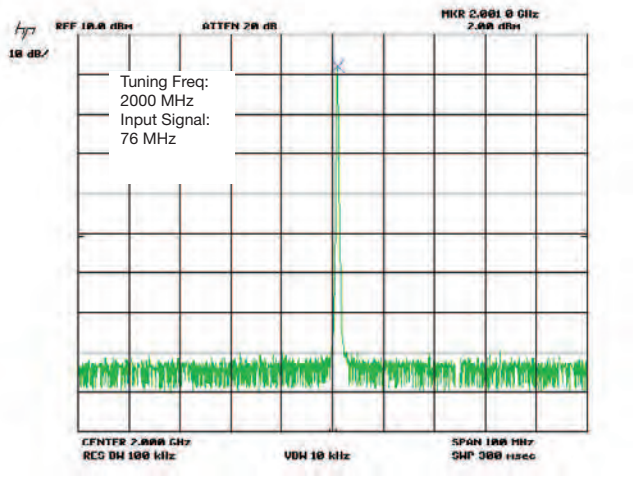


Figure 4: Up Converter Performance at 2000 MHz with 65 dB dynamic range

ADDED FEATURES THAT MAKE DTA-3200 AN ATTRACTIVE SOLUTION

RF Input/Output Switch Matrix: This enables a seamless scanning operation by enabling users to connect to multiple antennas (or power amplifiers) to enable frequency coverage up to 6 GHz.

Front-End LNA or Attenuator: The receiver input path architecture allows users to switch in either an LNA (for low signals) or a programmable attenuator (for a large-signal scenario). This allows users to make a Noise Figure vs. IP3 trade-off and prevent saturation of amplifiers and mixers in the presence of large signals.

LNA Out and Pre-Amp In Ports: The front-end LNA output and the Pre-amp inputs are externally accessible for handling variety of inputs and adding customized filtering.

Digital Programmable Attenuators: Up to three programmable attenuators (1 dB steps) are available for users to calibrate gain over the 6 GHz frequency range of operation. These attenuators are also used for programmable gain control.

ADVANCED CONTROL

Control of the DTA-3200 is over a 1 GbE link. The controller features a Virtex 5 FPGA and can be easily customized to implement direct control. The FPGA is also connected to 14 user I/Os that can be customized to serve as direct control. Some of the custom control options are:

- **Advanced automated scanning function by means of a scan table that defines the scan frequencies and dwell time**
- **Custom control by means of the user I/O**
- **External indication of synthesizer lock detect on the user I/O port**
- **On-board storage of calibration/configuration parameters and automatic configuration of the RF channels at power-up**

OPTIONAL INDEPENDENTLY TUNED CHANNELS

The DTA-3200 can also be offered with independent tuned RF up and down conversion channels. In this mode, additional synthesizer modules are added and each synthesizer drives a single UCON or DCON channel. This version is the DTA-3200 and can accommodate up to four channels in a 4U chassis height. Alternatively, the user may also use multiple DTA-3290 to obtain multiple independently tunable channels.

CUSTOMIZATION

D-TA can offer limited customization of DTA-3200 to meet special requirements, including IF, bandwidth, repackaging and ruggedization, and reduced frequency coverage to lower cost. Please contact factory.

RELATED PRODUCTS

The DTA-3200 works hand in hand with the DTA-2300, the multi-channel synchronized IF transceiver unit. The IF input and output signals of the DTA-3200 are fully compatible with the DTA-2300 and no additional amplification or filtering is required to interface with the DTA-2300. This is an enormous benefit for fast and simple system integration.

The DTA-3200 acts as ideal RF front end for the 10G/R series recorders that can record and play back signals in real time. A single record/playback system can handle up to four synchronized channels each at bandwidth of 40 MHz.

OPTIONAL TRAINING

Hands-on interactive training is offered either in our fully equipped Training Center or at the customer's facility. The Training Center boasts a fully equipped conference room and a dedicated Training Laboratory with access to D-TA products, as well as test equipment like oscilloscopes, spectrum analyzers, network analyzers and signal generators. The hands-on training covers a full discussion of the SDK structure, detailed product discussions and actual example application development with actual equipment. RF Systems design topics are also covered, including Noise Figure, IP3 and their impact on system sensitivity; RF Measurement techniques; RF System troubleshooting of intermodulation products, spurious signal generation, etc.; and RF mixer system details and impact of a mixer on intermodulation and spurious signals.

ORDERING INFORMATION

PART NO.	DESCRIPTION	REMARKS
DTA-3200S-xRT	Synchronized Multi-channel (x channels) RF up and down converter. Also offered in Receive ('R) or Transmit ('T') only Version	
DTA-3200H-xRT	DTA-3200 Configured for the HF Band (2MHz – 30 MHz)	
DTA-3200M-xRT	Independent tunable multi-channel (xx channels) RF up and down converter. Also offered in Receive ('R) or Transmit ('T') only Version.	
SDK-3200	Full source code SDK for DTA-3200	

DTA-2300

MULTI-IF DIGITAL TRANSCEIVER (SOFTWARE RADIO)

DTA-2300 is designed for applications that require a large number of inputs and outputs (antenna channels), high precision and large bandwidths. DTA-2300 supports up to 16 receive and transmit channels in a 1U enclosure. Each channel includes a 16-bit, 130 MSPS ADC (160 MHz version also offered) for receive and a 16-bit 500 MSPS interpolating DAC for transmit. Each group of four channels is connected to a large Xilinx Virtex 5 (SX95T) FPGA. Each FPGA is loaded with D-TA's standard DDC (Digital Down Conversion with programmable decimation) core and 10 Gigabit Ethernet MAC and logic for implementing UDP/IP protocol. The high data transfer rate capability of the 10 Gigabit network allows real-time transfer of large bandwidth data (over 100 MSPS sample rate for each channel) for server-based processing. A separate Master FPGA is used for control via the 1 Gigabit Network.

DTA-2300 offers fully synchronous operation for phase-coherent applications. Each ADC and DAC sample clock can be independently delayed in steps of 10 ps for calibrating any RF and/or cable mismatch. The DTA-2300 is supported by DTA-3200 Tunable RF Front end, DTA-5000 Record/Playback and DTA-1000 Server systems for Multi-Core processing aided by the D-TA Software Development Kit, application development support and training.

[Download Tech Notes TN-5 and TN-12 for more information on DTA-2300]

AT A GLANCE

- Up To 16 Receive & Transmit Channels
- 16-Bit, 130 MHz ADCs & 16-Bit, 500 MHz DACs
- Fully Synchronous Operation
- Programmable Sample Clock Delays in 10 ps Steps for Calibration
- Multi-Unit Synchronization
- Up To 4 Large Virtex 5 FPGA for Data and 1 Master FPGA for Control
- Up To 4 10 Gigabit Networks (XFP, Optical) for Data
- 1 GbE Networks for Control
- Optional 1 GbE Network for Data
- Optional Expansion Card for Additional FPGA Resources
- Flexible Clocking Options – Internal (TCXO) or External Reference Clock
- Data Time Stamping with 6.4 ns Resolution

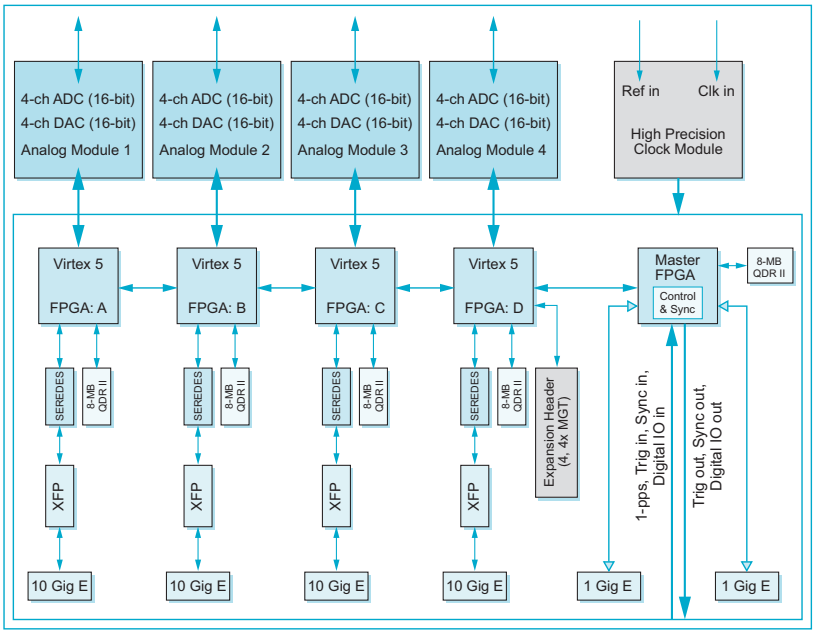
APPLICATIONS

- Phased Array Radar
- SIGINT /COMINT /DF
- MIMO Radio / Radar
- Arbitrary Waveform Generation
- Cognitive Radio
- Mobile & Satellite Systems
- TDOA Geolocation

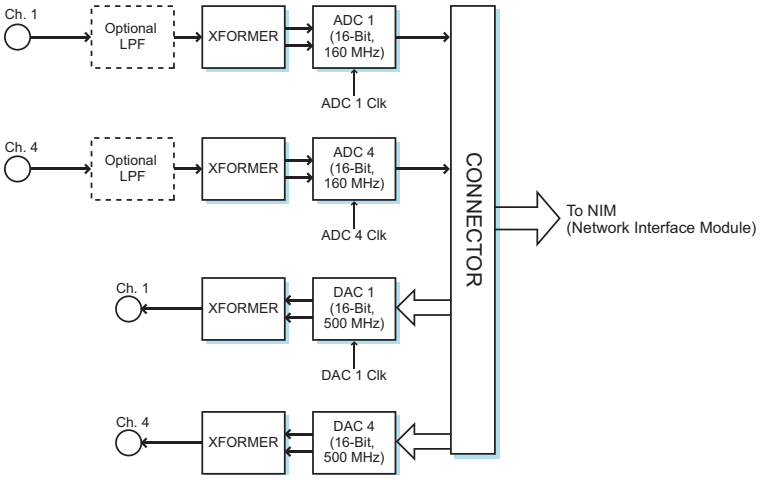
DTA-2300 (1U X 19" X 24")

The DTA-2300 consists of up to four Analog Interface Modules (AIMs), a High Performance Clock Module (HPCM) and a Network Interface Module (NIM). The HPCM offers flexible clocking options: the ADC and DAC clocks are supplied by the highly stable internal TCXO; the VCO locks to the internal TCXO or an external reference input (10 MHz – 100 MHz), and ADC and DAC clocks are generated by dividing down VCO clock; ADC and DAC clocks are supplied from CLK IN 1 input; or ADC and DAC clocks are separately supplied from CLK IN 1 and CLK IN 2 inputs. The clocks to each ADC and DAC can be independently delayed in steps of 10 ps for phase adjustment or calibration.

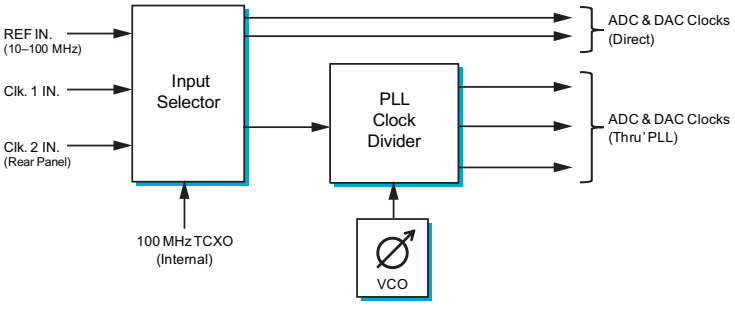
DTA-2300 System Architecture



Analog Interface Module (AIM)



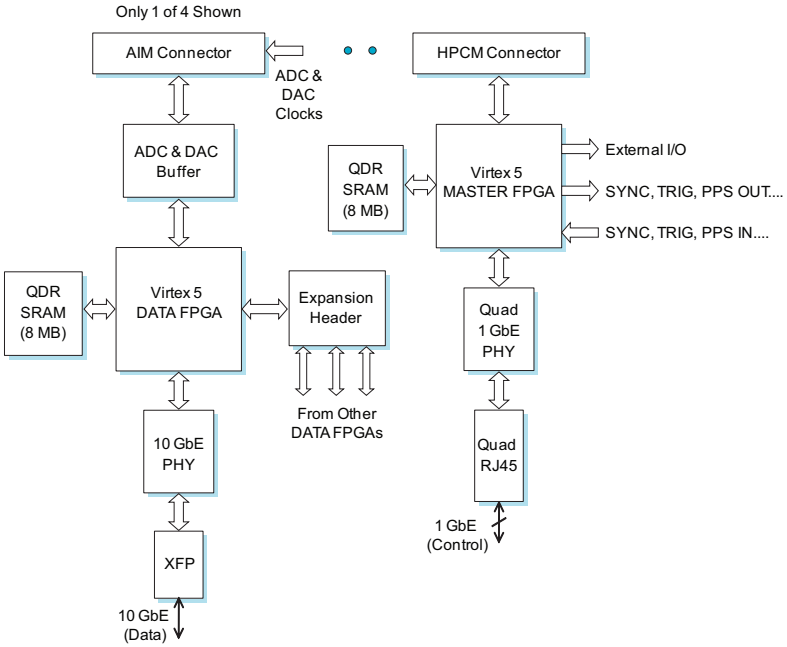
High Performance Clock Module (HPCM)



Network Interface Module (NIM)

The NIM module includes four large data FPGAs and a Master FPGA for control. Each FPGA is connected to 8 MB QDR-II SRAM. Each of the data FPGAs connect to a 10 GbE interface via a XFP module (for using multimode fiber-optic cable). The Master FPGA supports two 1 GbE interfaces for optional redundant control interface. Each Data FPGA receives six ADC channel data: four from its own AIM and two other additional ADC channels from other AIMs. Each FPGA, however, provides data only to its own DACs. The FPGAs are connected to one another via GTP links and an LVDS bus for high-speed inter-FPGA data transfer to allow shared processing.

The FPGAs implement a UDP/IP protocol over the 10 GbE and 1 GbE interface. The data over the 10 GbE interface is packetized and has a D-TA header containing important information that allows the user to easily access and process the data. Each 10 GbE interface sustains data rate in excess of 800 MBytes/s to a commercially available server-class computer. The DTA-2300 supports Ethernet Jumbo frame (up to 9000 bytes) over the network interface.

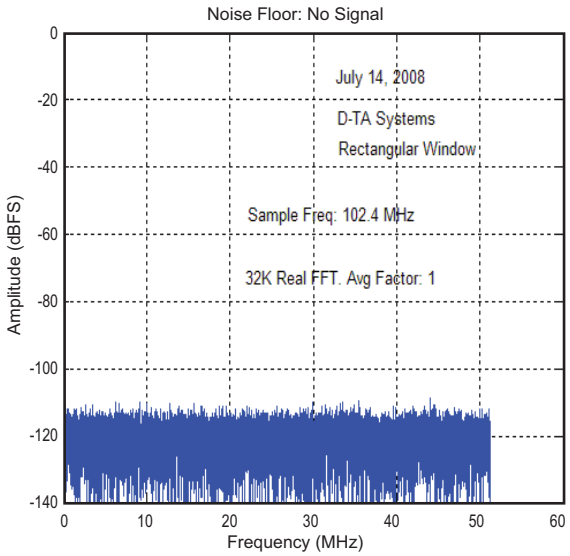


10 GbE DATA PACKET STRUCTURE

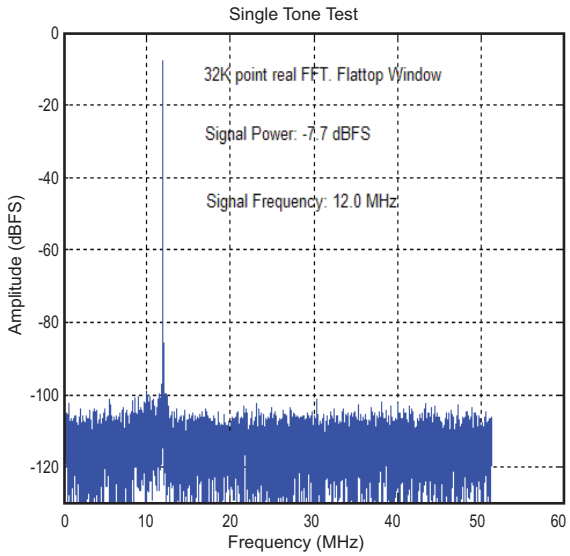
The packet header includes the model serial number, a packet ID (a 16-bit packet counter), a Trigger Coarse Time (count of a 32-bit counter incremented by internal or external pps pulses), a Trigger Fine Time (count of a 32-bit counter incremented by the FPGA fabric clock and reset by the pps pulse), operating mode (continuous, one shot, etc.) and the number of samples for each of the channels in the Ethernet packet. When a Trigger is applied (external or software), the Trigger Coarse Time counter is reset by every occurrence of the Trigger.

START BIT	BITS [31:16]	BITS [15:0]
0	DTA MODEL NUMBER	PACKET ID
32	TRIGGER COARSE TIME	
64	TRIGGER FINE TIME	
96	USER FIELD	OPERATING MODE
128	RESERVED	
160	NO. OF SAMPLES FOR CH. A	NO. OF SAMPLES FOR CH. B
192	NO. OF SAMPLES FOR CH. C	NO. OF SAMPLES FOR CH. D
256	NO. OF SAMPLES FOR CH. E	NO. OF SAMPLES FOR CH. F
.....	CHANNEL DATA AS PER CHANNEL MAP	
....	CHANNEL DATA AS PER CHANNEL MAP	

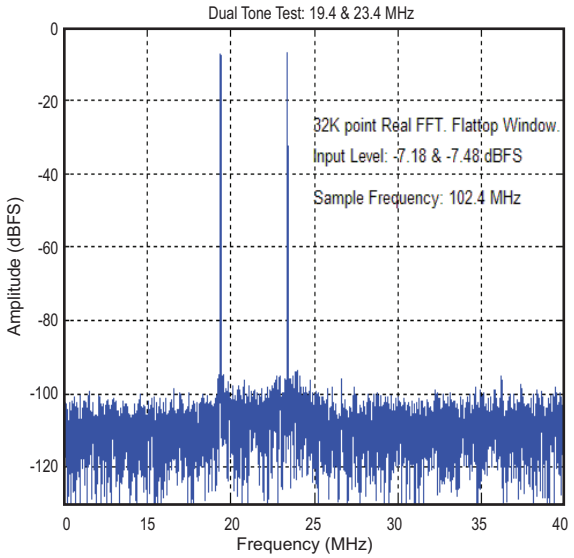
ADC & DAC Performances



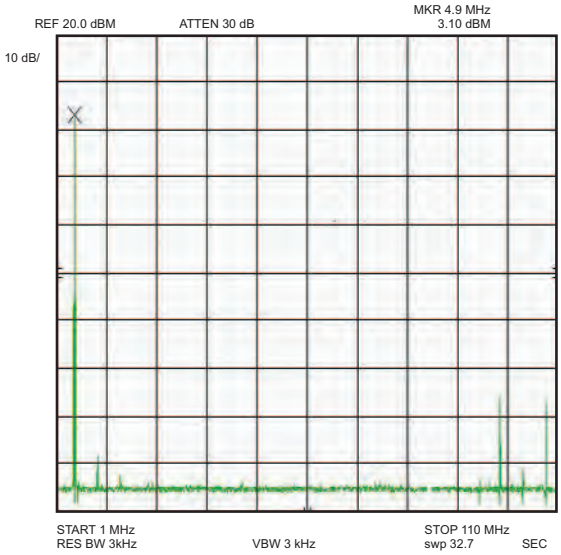
ADC Noise Floor (No. Input)



ADC Single Tone Performance



ADC Dual Tone Performance



DAC Single Tone Performance

ADC AND DAC OPERATION

The ADCs provide a very large input bandwidth and a wide dynamic range. The maximum sampling rate is 130 MSPS (optionally 160 MSPS) and the minimum sampling rate is 32 MSPS. The DAC (TI DAC5687) chip is a dual channel interpolating DACs with 500 MSPS output rate. Each DAC chip offers two real channels or one complex channel. Each AIM module provides four real output channels or two complex output channels. The DAC offers interpolation of 1 (bypass), 2, 4 or 8. The maximum input data rate is 160 MSPS and the minimum data rate is 20 MSPS. The user typically provides input to the DAC at the input data rate, and the DAC internally generates the output rate clock depending on the interpolation chosen. The DACs can be operated in the Complex Up-converting mode where the input data is up-converted to an Intermediate frequency. The DAC can also be operated as Real Direct or Real Interpolating DAC. In the Real Interpolating mode, it is possible to do up-conversion by selecting high-pass filtering (instead of low-pass filtering) following interpolation. The D-TA SDK supplied with DTA-2300 shields the user from having to learn the intricacies of the devices.

[Download Tech Notes TN-6, TN-7 and TN-13 for more information on DTA-2300 analog performances]

DDCS AND DUCS

Each DTA-2300 Data FPGA is pre-loaded with a Digital Down Converter (DDC) core for each ADC channel. The DDC offers programmable decimation of 2, 4, 8, 16 and 32. Each DDC has a programmable NCO that allows basebanding (centered on DC) of an IF signal following sampling. The IF signal is typically undersampled, in which case the ADC sample clock frequency must be carefully selected. The DTA-3200 RF Front End provides a 75 MHz IF and a 40 MHz BW with a 5 MHz guard band on both sides. This IF signal is conveniently undersampled using a 100 MHz clock.

The DDC operation illustrated here results in a spectral flip following undersampling. The signal spectrum is first shifted to DC by properly selecting the NCO frequency and then filtered and decimated to obtain the desired processing bandwidth. A more detailed discussion on the architecture of the DDC can be found in the Firmware Development section of this catalog.

The DTA-2300 uses the TI DAC5687 dual DAC chips that can offer two real outputs or 1 complex output per DAC. The DAC chip has built-in Interpolation (1, 2, 4, or 8) and digital up conversion functions. The DAC can be operated as a conventional DAC without up-conversion, with or without Interpolation. In the complex mode, up conversion to a IF frequency is performed following interpolation to increase the output rate (DAC Clock Rate) to Input Data Rate (Fi) X Interpolation Factor, as illustrated here. The output clock is generated by the DAC based on the Interpolation Factor. In the real mode, up conversion is also possible, however, this mode of operation does not allow arbitrary selection of the IF (up conversion center freq.).

Illustration of the DDC operation

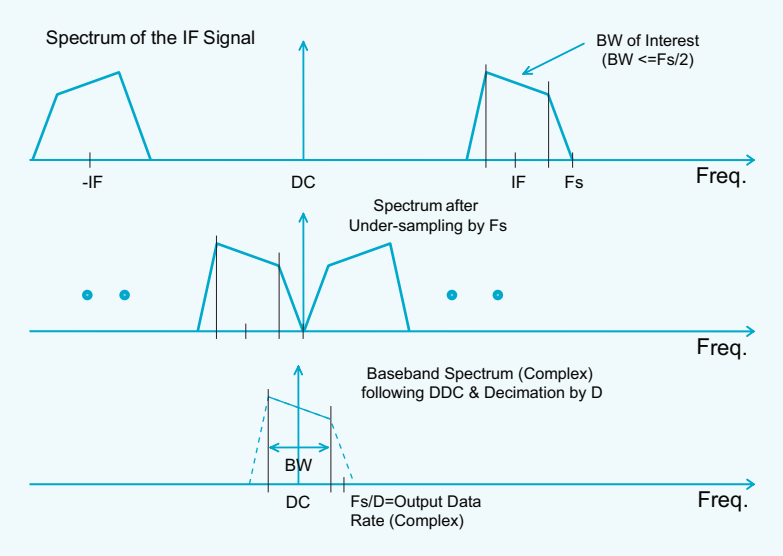
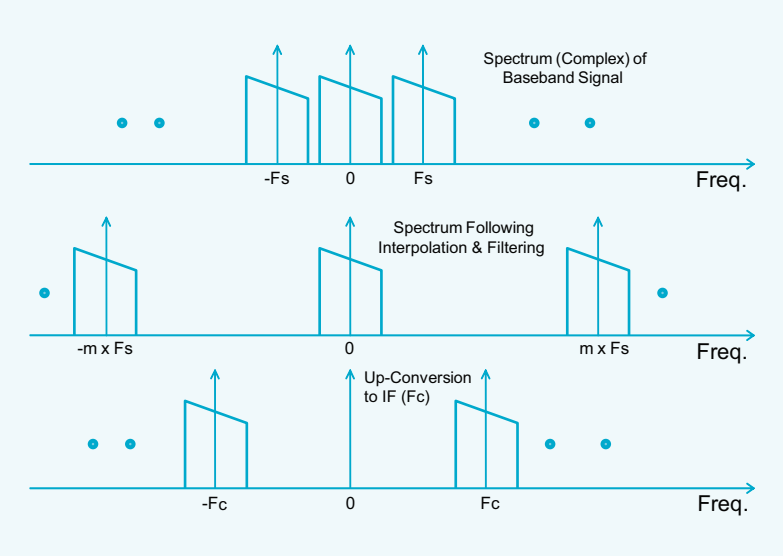


Illustration of the DUC operation



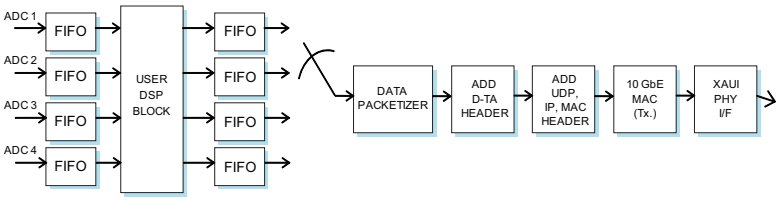
MAJOR FEATURES

FEATURE	VALUE	COMMENTS	FEATURE	VALUE	COMMENTS
No. of ADC Channels	Up to 16	In Groups of 4	No. of DAC Channels	Up to 16	In Groups of 4
Maximum/ Minimum Sample Rate (LTC 2208)	130 MHz/32 MHz	Also Available in 160 MHz Version (LTC 2209)	Maximum/Minimum DAC Input Data Rate (TI DAC 5687)	130 MHz/32 MHz	Max. Output Rate is 500 MHz
ADC Precision	16 Bits		DAC Precision	16 Bits	
Full-Scale Input	+5.5 dBm	Into 50 Ohm	Full Scale Output	+3 dBm	Into 50 Ohm
Input Coupling	AC Coupling (transformer)	A DC Blocking Capacitor Present	DAC Interpolation Factor	1, 2, 4, 8	
Input 1 dB	1 MHz to 300 MHz		Output Impedance	50 Ohm	
Input Connector	50 Ohm SMA Female		Output Connector	50 Ohm SMA Female	
ADC SFDR	-90 dBFS	Typical	DAC SFDR	-75 dBFS	Typical
ADC 2-Tone IMD	-90 dBFS	Typical	DAC 2-Tone IMD	-70 dBFS	Typical
TCXO Clock Phase Noise	<-100 dBc/Hz @100 Hz <150 dBc/Hz @10 kHz				
	Internal 100 MHz TCXO Clock	Standard Data FPGA Core	DDC with Programmable Decimation of 2, 4, 8, 16, 32	Contact factory for other options	
Dimensions	19"(W) X 24"(D) X 1.75"(H)	Weight is 15.4 lbs (7 kg)	Power	300 Watts Max. (fully populated)	110V or 220V Operation

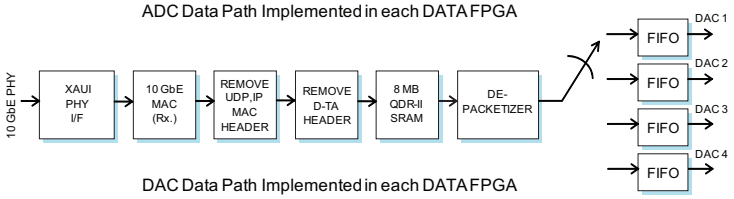
FPGA FIRMWARE PROGRAMMABILITY

The four Data FPGAs in the DTA-2300 can be used for implementing DSP functionality. D-TA provides an optional Firmware Development Kit (FDK) to enable users to develop their own custom functionality. The FDK includes the full source HDL code for D-TA logic as well as ucf for the device. The user can develop application-specific FPGA cores and load the FPGAs over the GbE interface. The ADC and DAC data paths are implemented in the FPGA to allow the user to only develop the DSP core and reuse the data transfer logic already developed by D-TA Systems. Note that the DDC core supplied with the DTA-2300 is implemented in the User DSP Block.

[Download Tech Note TN-10 for more information on DTA-2300 FPGA programming]



ADC Data Path Implemented in each DATA FPGA



DAC Data Path Implemented in each DATA FPGA

DTA-2300 CONFIGURATIONS

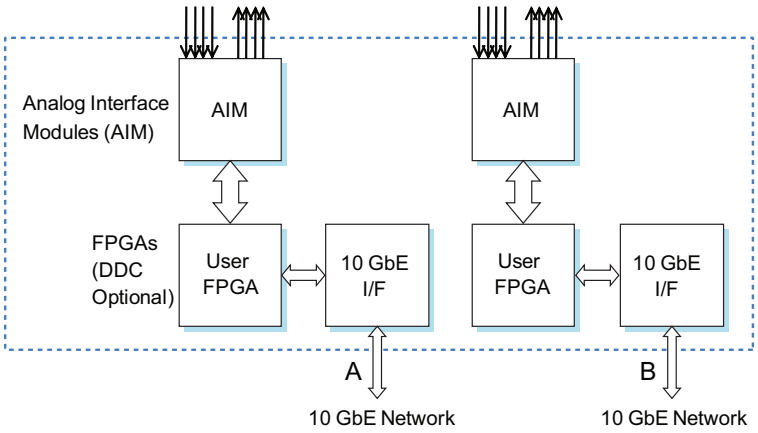
DTA-2300 is available in three different versions.

The DTA-2300D version (-yRT-pFn, where y represents the number of receive and transmit channels, p is the number of FPGAs, and n represents the number of 10 GbE networks) offers up to two (one for each AIM) free FPGAs for user programming. The maximum input and output channel count is eight if two AIMs are used. Since each 10 GbE network can sustain over 800 MBytes/s throughput rate, the "D" can support 40 MHz BW (100 MHz sampling rate) for each channel for real-time data transfer to the host computer.

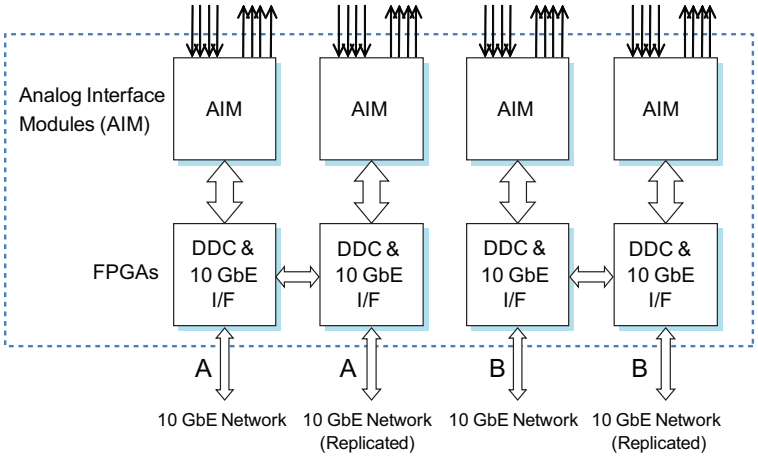
The DTA-2300M version offers up to two replicated 10 GbE networks (two identical networks) by merging data from two FPGAs. The replicated ports offer the advantage that two different processing (e.g, recording and signal processing) can be done simultaneously on the same data. The "M" version is available for up to 16 channels. For channel count up to eight, the supported BW is 40 MHz for each channel for real-time data transfer to host computer. For 16 channels, the BW is 20 MHz.

The DTA-2300S version is available for up to 16 channels. This configuration uses all four 10 Gigabit networks and supports 40 MHz BW for all channels.

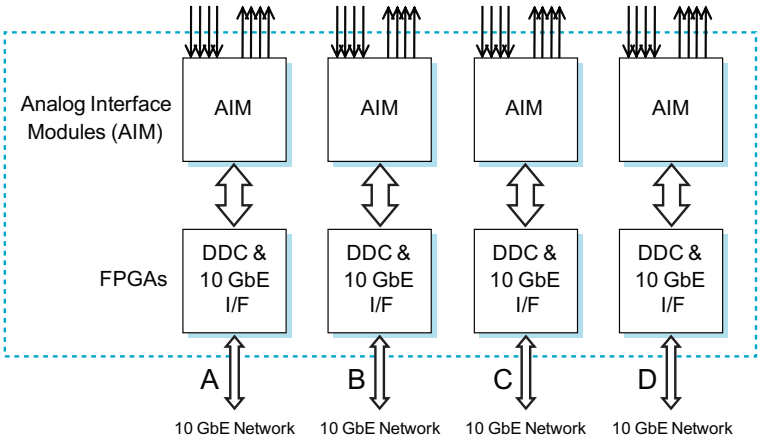
DTA-2300D-8RT-4F2



DTA-2300M-16RT-4F4



DTA-2300S-16RT-4F4



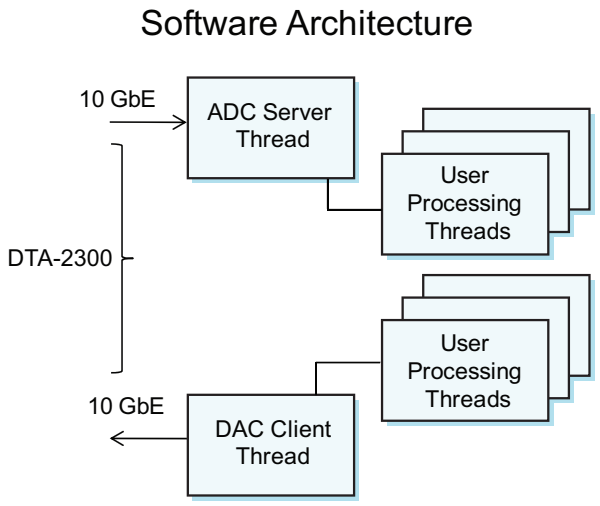
MULTI-CORE SOFTWARE PROCESSING

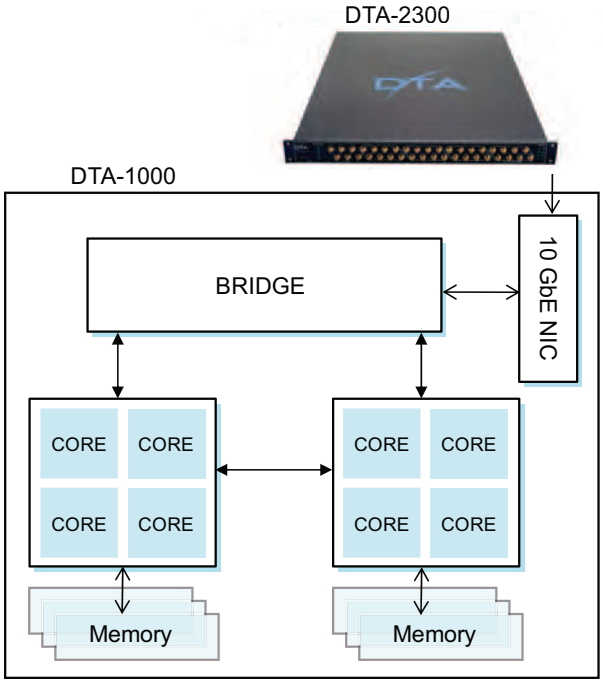
Today's server-class computers offer significant processing power (multiple processors running at multi GHz rates) that can be harnessed using D-TA's Software Development Kit (SDK). For users' convenience and speedy deployment, D-TA offers DTA-1000, a high-performance quad core dual Xeon server (1U) integrated with the Network Interface Card (NIC) and SDK. The system uses Linux OS (kernel 2.6.26) with real-time patch.

The SDK consists of a Control SDK, Data SDK and Optional Real Time Processing modules. The SDK is written in POSIX-compliant C++ code (full source code). The Control SDK contains all APIs for control and abstracts the need for users to understand register structure of the device in detail. The Data SDK allows abstraction of data transfer to and from DTA-2300 and allows the user to concentrate on application development.

For multi-channel and large bandwidth signal processing, multiple servers – one for each 10 Gigabit fibers (network) – can be used. One of the key features of the DTA-2300 is that it maintains synchronization across fibers for both input and output operations.

[Download Tech Notes TN-14 and TN-17 for more information on software processing]





RECORD AND PLAYBACK AND RF FRONT END

D-TA offers the most powerful recording and playback solutions using the DTA-5000 server-based RAID storage system. Using all 4 DTA-2300 fibers and four DTA-5000 units, D-TA is able to record and play back at rates over 3.2 GBytes/s. This means that 16 radio signals with 40 MHz BW each can be recorded or played back simultaneously in a phase-coherent fashion. DTA-2300 is also supported by the DTA-3200 Tunable RF/IF Transceiver, which offers 40 MHz instantaneous bandwidth, 75 MHz IF (to provide optimum under sampling with 100 MHz clock) and phase-coherent operations.

[Download Tech Notes TN-11, TN-17 and TN-18 for more information on D-TA's end-to-end multi-antenna software radio solution]

MULTI-UNIT SYNCHRONIZATION

The DTA-2300 is designed for synchronous phase-coherent operation across a large number of antenna channels. The ADC and DAC clocks and Trigger signals can be generated in the Master DTA-2300 system and transmitted to other slave systems. Any delays due to buffers and varying cable lengths can be calibrated by adjusting the programmable sample clock delays for each ADC and DAC independently.

HANDLING LARGER BANDWIDTHS

The DTA-2300 ADCs can be operated in a multiplexed fashion to simulate a higher sampling rate. For example, if two ADCs are operated with sample clocks that are 180° shifted in phase and both ADCs are supplied with the same signal, this effectively results in doubling the sample rate. Any error in achieving precisely 180° phase shift between the clocks results in spurs. The DTA-2300 provides independent adjustment (by software means) of each sample clock delays in steps of 10 ps. This feature can be used to achieve the desired 180° phase shifts.

OPTIONAL DATA TRANSFER OVER 1GbE INTERFACE

For some applications involving very narrow band signals (e.g., COMINT, SIGINT, communications), the data rate is so low that a 1 GbE link is adequate. This enables the removal of the 10 GbE logic and implement data transfer over the 1 GbE interface. DTA-2300 has the capability for implementing additional 1 GbE link so that users can separate the data and control links over separate 1 GbE link for easy system architecting.

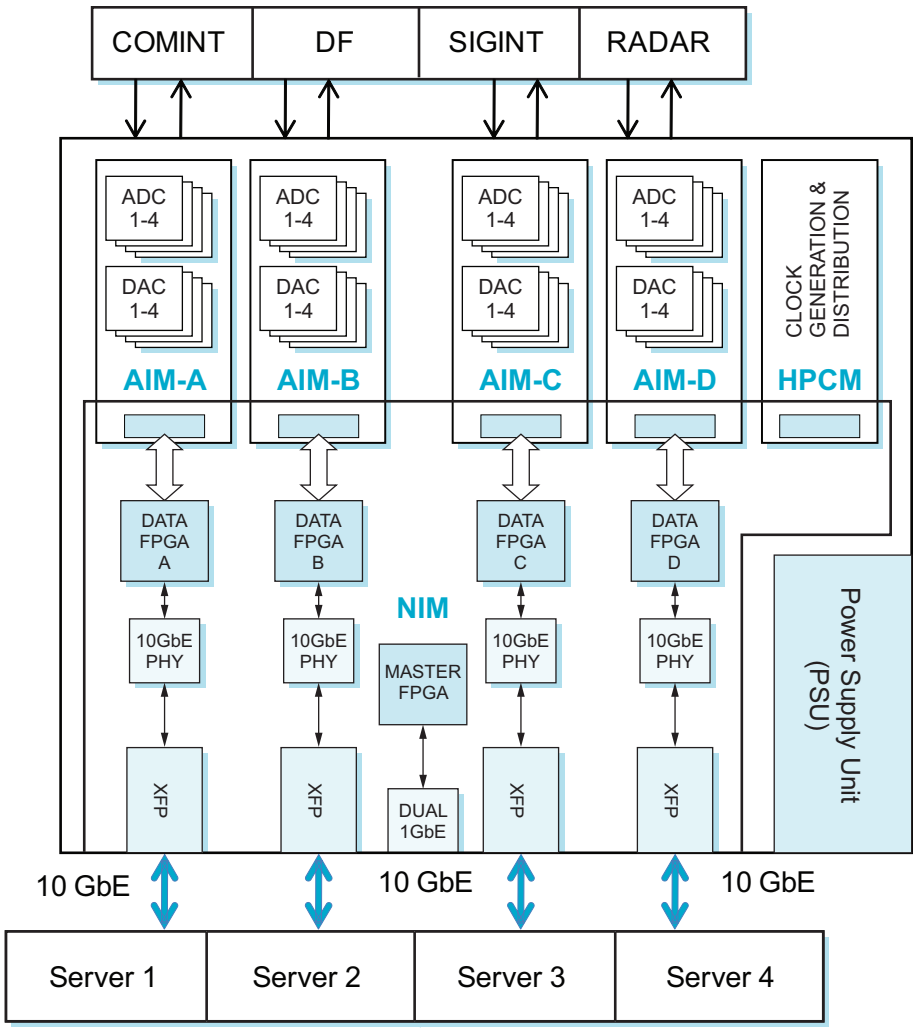
EXPANDING THE CAPABILITY OF DTA-2300

The DTA-2300 is an extremely flexible platform that can be easily customized to suit specific user requirements. The simplest is adding additional DSP or other functionality in the four large data FPGAs (Virtex 5, SX95T devices). The DTA-2300 is also equipped with expansion header that enables additional daughter card to be added to the DTA-2300. The expansion header is directly connected to each of the four data FPGAs with a full duplex 10 Gbps link. The expansion header also features the capability to implement additional 1 GbE links for direct command and control. A customized FPGA-based daughter card can thus be directly connected to each of the data FPGAs, thereby increasing the available processing power. D-TA can easily provide customized daughter cards for such capability expansion.

ORDERING INFORMATION

PART NO	DESCRIPTION	COMMENTS
DTA-2300X-yRT-pFn	Digital IF Transceiver Version X=S, D or M; and y No. of Channels (if receive only, T is omitted; p is the no. of Data FPGA and n is the no. of 10GbE networks)	SDK and FDK are optional items
SDK-2300	Software Development Kit	
FDK-2300	Firmware Development Kit	
DTA-1000	1U Dual Quad-Core Server with 10 GbE NIC and SDK Pre-installed	
Training	Software and Firmware Development Support and Training, Customization, Acceptance Test Plan, etc.	Contact factory

RUNNING MULTIPLE APPLICATIONS SIMULTANEOUSLY WITH DTA-2300



RUNNING MULTIPLE APPLICATIONS SIMULTANEOUSLY WITH DTA-2300

The DTA-2300 Multi-Antenna Digital IF Transceiver can be configured for multitudes of software radio and radar applications. The DTA-2300 can also run multiple applications simultaneously. For applications requiring less than eight antennas, two or more applications can be run concurrently. The assumption is that the sample clocks are the same for all applications, and the processing bandwidth for each group is defined by appropriately programming the corresponding DDCs.

The 10 Gigabit output network for each application is connected to a different server for running its own application. This capability of the DTA-2300 offers significant cost and space savings for many critical applications.

[Download Tech Note TN-08 for information on a Precision RF Direction Finding technique]

DTA-5000

10 GIGABIT RECORD & PLAYBACK SYSTEM

DTA-5000 is an extremely scalable and ultra-fast 10 Gigabit record and playback system. It is designed to work with D-TA sensor signal acquisition products that are 10 Gigabit (10GbE) network attached. The DTA-5000 can also work with third-party products that provide a 10 GbE UDP/IP network for data transfer. The DTA-5000 includes a Multi-Core server, a 10 Gigabit Network Interface Card (NIC) and 16 high-reliability SAS disk drives. Each disk has either 300 GByte or 600 GByte capacity. The total capacity, therefore, is either 4.8 or 9.6 Terabytes. The record/playback design is based on highly optimized multi-threaded software operating under Linux OS with real-time patch.

The sustained record/playback rate per DTA-5000 (per 10 GbE network) is over 800 MBytes/s. Multiple DTA-5000 systems can be used with multiple 10 GbE networks to linearly increase the throughput rate. The DTA-5000 is packaged with D-TA products to offer a complete record and playback solution for radio/radar and sonar/acoustic applications. The 10Gx series products (where x denotes the number of 10 GbE networks, x=1, 2 or 4) comes with a comprehensive GUI or optional control API for fail-safe operation.

[Download Tech Notes TN-11, TN-18 and TN-25 for more information on D-TA's Record & Playback solution]

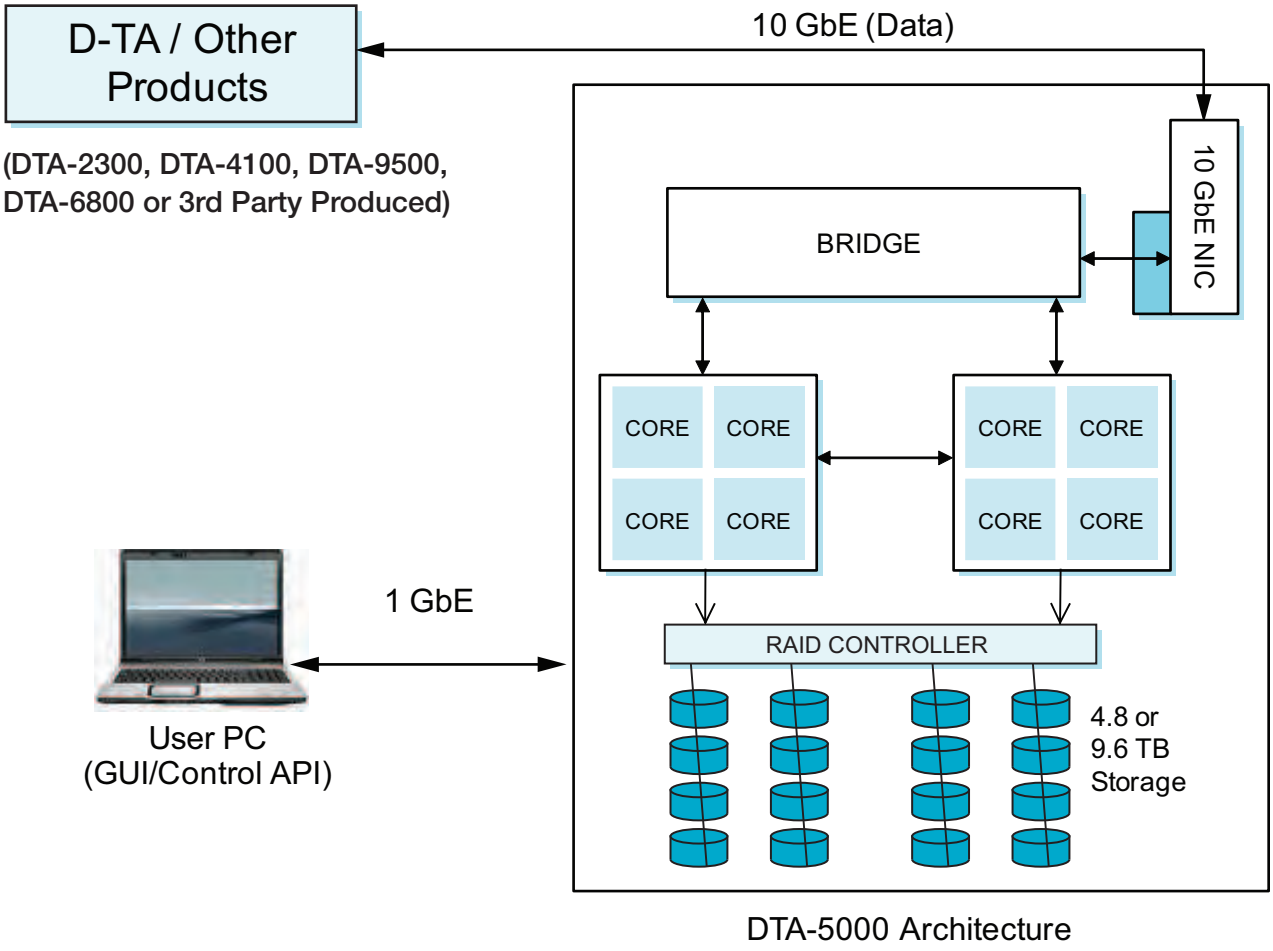
AT A GLANCE

- System Based on Commercially Available RAID Storage System With Up To 16 High-Reliability SAS Drives
- Storage Capacity Up To 9.6 Terabytes
- Real-Time Multi-Core Software Based Design
- Record & Playback At Rates Over 800 MBytes/s Per 10 Gigabit Network & DTA-5000
- Scales Linearly As More Networks And DTA-5000 Systems are Added
- Synchronized Operation Across Multiple Networks Packaged with D-TA Radio & Acoustic Products (10Gx Series) to Offer Complete Record / Playback Solution (3rd Party Products with 10 GbE UDP/IP Network can also be supported)
- Comprehensive GUI or Control API for Failsafe Operation for the 10 Gx Series Products
- A Rugged Version DTA-5000R is also Available

APPLICATIONS

- Phase-Coherent Recording / Playback of Wideband Radio & Radar signals with DTA-2300 or DTA-9500
- Multi-Channel Sonar / Acoustic Signal Recording / Playback With DTA-4100
- Arbitrary Waveform Generation for RF Test
- Scenario Generation
- Sonar / Acoustic Simulator & Stimulator

DTA-5000 [3U(H) X 19"(W) X 26"(D)]



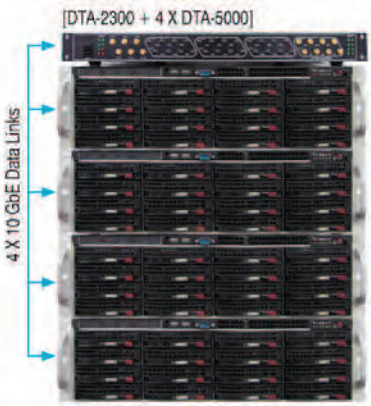
DTA-5000 Architecture

SCALABLE CONFIGURATION

Rate >800 MBytes/s

Rate >1.6 GBytes/s

Rate >3.2 GBytes/s



10G1-2300

- Sustained Record / Playback Rate: >800 MB/s
- Max. Storage Capacity: 4.8 or 9.6 TB

10G2-2300

- Sustained Record / Playback Rate: >1.6 GB/s
- Max. Storage Capacity: 9.6 or 19.2 TB

10G4-2300

- Sustained Record / Playback Rate: >3.2 GB/s
- Max. Storage Capacity: 19.2 or 38.4 TB

10 GIGABIT PACKET STRUCTURE

The 10G series record/playback systems that use one or more DTA-5000 system(s) with a D-TA sensor interface product(s) typically use a data packet structure with the following characteristics:

- **UDP/IP with a IP datagram size close to 57,670 bytes**
- **Ethernet Jumbo frame (size close to 8266 bytes)**
- **Single source and single destination (destination is DTA-5000)**
- **Data parsing and IP-based data filtering are not used**

The PACKET ID field in the header is incremented every packet and is an easy way to check data continuity. The other fields in the header allow users to read and process the data easily by storing all essential information as part of the data packet.

BITS [31:16]	BITS [15:0]
DTA MODEL NO	PACKET ID
TRIGGER COARSE TIME	
TRIGGER FINE TIME	
USER FIELD	OPERATING MODE
RESERVED	DATA FORMAT & NUMBER OF IP PER UDP
CH A NUMBER OF SAMPLES	CH B NUMBER OF SAMPLES
CH C NUMBER OF SAMPLES	CH D NUMBER OF SAMPLES
DATA (CH A)	DATA (CH A)
DATA (CH A)	DATA (CH A)
DATA (CH B)	DATA (CH B)
DATA (CH B)	DATA (CH B)
.....	.....

GRAPHICAL USER INTERFACE (GUI)

The 10G series products come with a comprehensive and intuitive GUI that is designed for fail-safe operation. The GUI resides on the user's PC and allows easy control of all system components. The GUI provides status information, disk capacity and snapshots of Time or FFT displays for data quality check during record and playback. The recording can be stopped manually or continue for a programmed duration or size. Any selected run or portion of run can be played back. Pause and loop functionalities are supported.

THE MAJOR GUI FEATURES ARE:

- **Tabbed for ease of navigation and grouping of functions**
- **OS and system agnostic – Windows (XP, Windows 7), Linux, etc.**
- **Control of all system parameters (DTA-5000(s) and D-TA Sensor Interfacing and Processing Products)**
- **System status and disk status information**
- **Configuration can be saved in a file for future reload**
- **Record session management**
- **Programming record settings like session name, description, record by size, and record by duration**
- **Progress bar to indicate record/playback progress**
- **Time series or FFT snapshot display for data quality check during record or playback**
- **File transfer to remote storage device (over 1 GbE or 10 GbE link)**

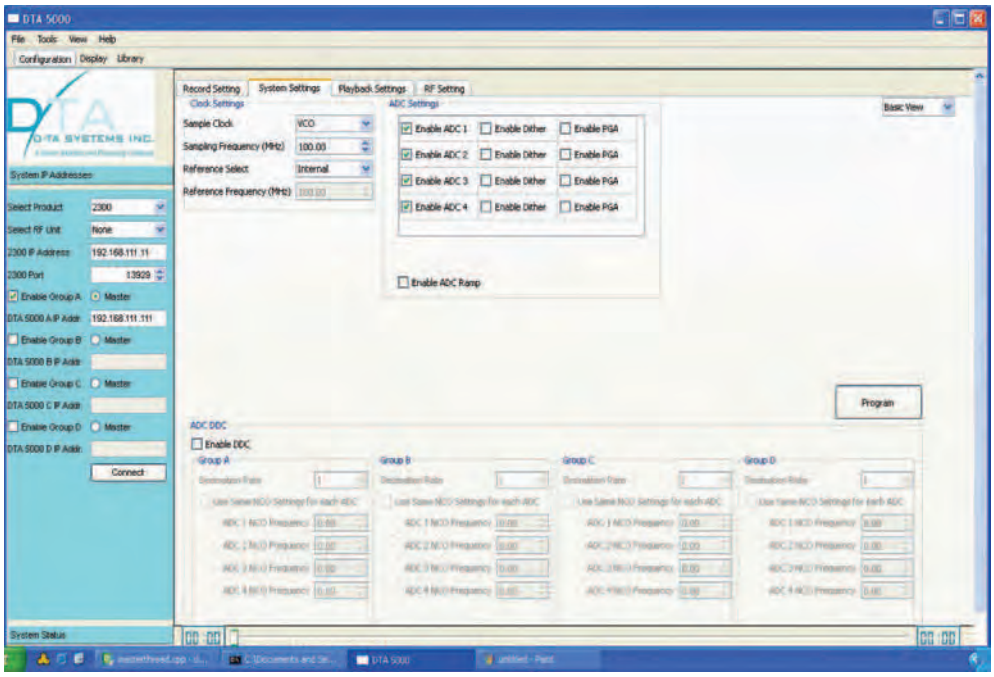
FILE STRUCTURE

The data is recorded in an XFS file system for easy access by Windows or other operating systems. Each recording session is broken into multiple small files for quick network access. Each file includes a header that includes all information for identifying and processing data in the file. The headed includes space for operator annotation. The list of recorded session is maintained in the library.

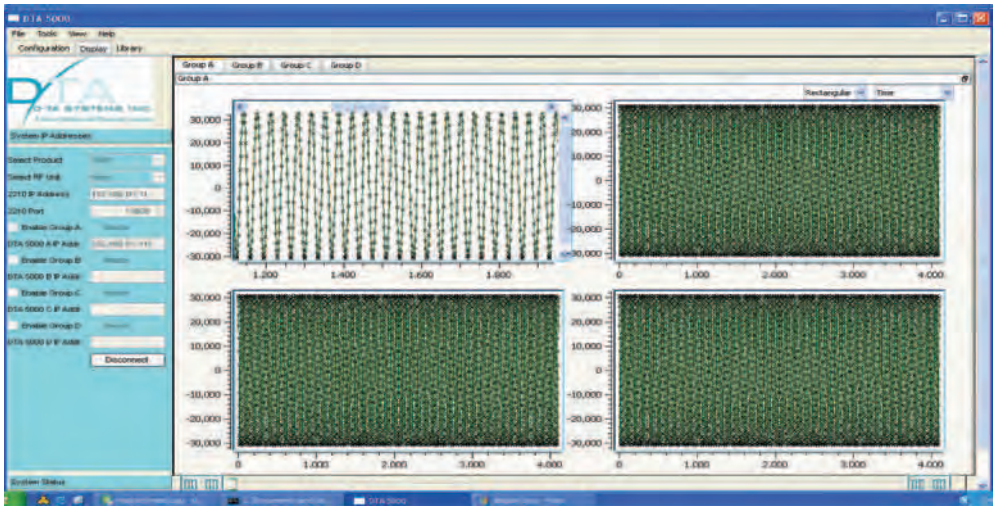
FILE TRANSFER

The GUI offers a file transfer functionality that allows users to transfer a full or partial recording session over the 1 GbE network to a remote computer. For fast transfer, a 10 GbE network connection may be created by routing the 10 GbE record link to the user network.

Configuration Screen (user PC) allows easy control of all systems



Display Screen (user PC) provides snapshot displays of FFT/Time data during record/playback



OPTIONAL CONTROL API

The DTA-5000 can be optionally provided with a C++ API that allows users to embed the control of the recorder in their applications and control the recorder from a remote device. The API is available for Windows 7, Windows XP or Linux. Sample API functions include dtaAPI: construct an API interface for DTA-5000; dtaRecord: initialize and prepare DTA-5000 for recording; dtastopmodules: stop recording; and dtaGetDiskStatus: retrieve disk quota status.

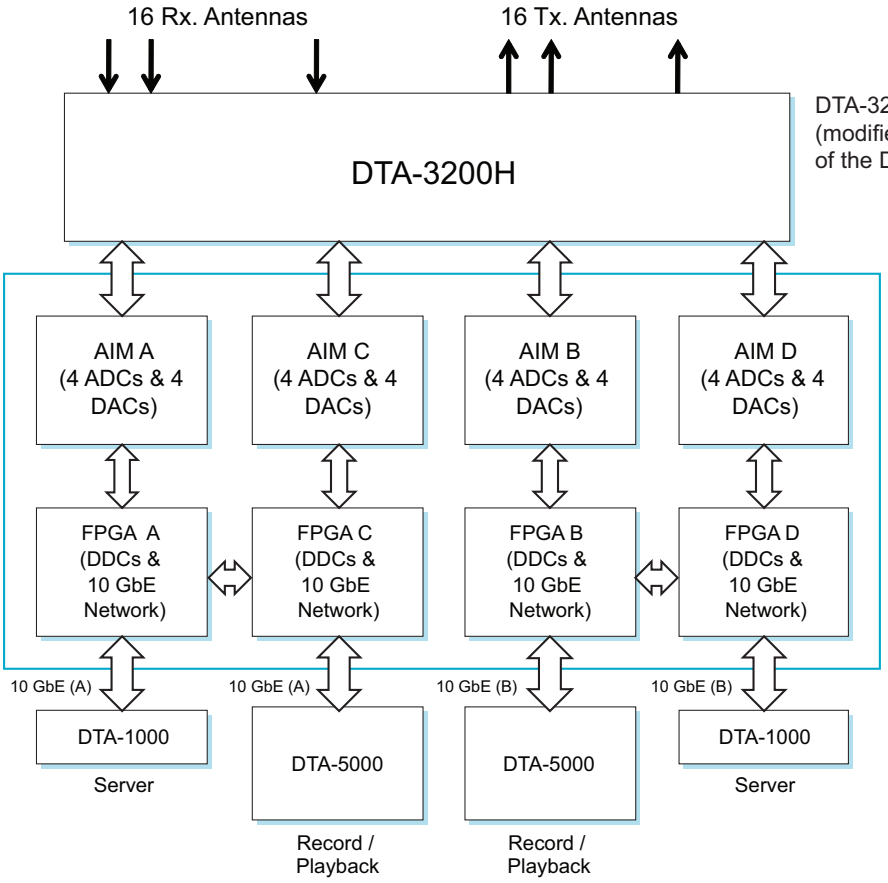
PLAYING BACK COMPUTER-GENERATED DATA

Aside from playing back pre-recorded data files, DTA-5000 can also be used to play back computer-generated data for arbitrary waveform generation, simulation and test. An optional MATLAB data generation utility is available that allows the user to generate digital data and transfer the same to DTA-5000 for playback.

ORDERING INFORMATION

PART NO.	DESCRIPTION	REMARKS
10G1- (Interface Product)	Record/Playback System with one 10 GbE Network and one DTA-5000 with 4.8 Terabyte total storage capacity	Interface Product: DTA-2300, DTA-4100 or DTA-9500. Record/Playback rate 800 MBytes/s.
10G1E- (Interface Product)	Record/Playback System with one (10 GbE Network and one DTA-5000 with 9.6 Terabyte total storage capacity	Record/Playback rate 800 MBytes/s
10G2- (Interface Product)	Record/Playback System with two 10 GbE Network and two DTA-5000s with 9.6 Terabyte total storage capacity	Record/Playback rate 1.6 GBytes/s
10G2E- (Interface Product)	Record/Playback System with two 10 GbE Network and two DTA-5000s with 19.2 Terabyte total storage capacity	Record/Playback rate 1.6 GBytes/s
10G4- (Interface Product)	Record/Playback System with four 10 GbE Network and four DTA-5000s with 19.2 Terabyte total storage capacity	Record/Playback rate 3.2 GBytes/s
10G4E- (Interface Product)	Record/Playback System with four 10 GbE Network and four DTA-5000s with 38.4 Terabyte total storage capacity	Record/Playback rate 3.2 GBytes/s

MULTI-ANTENNA HF PROCESSING



DTA-3200H uses only the direct band (modified for 2 MHz to 30 MHz operation) of the DTA-3200 RF system.

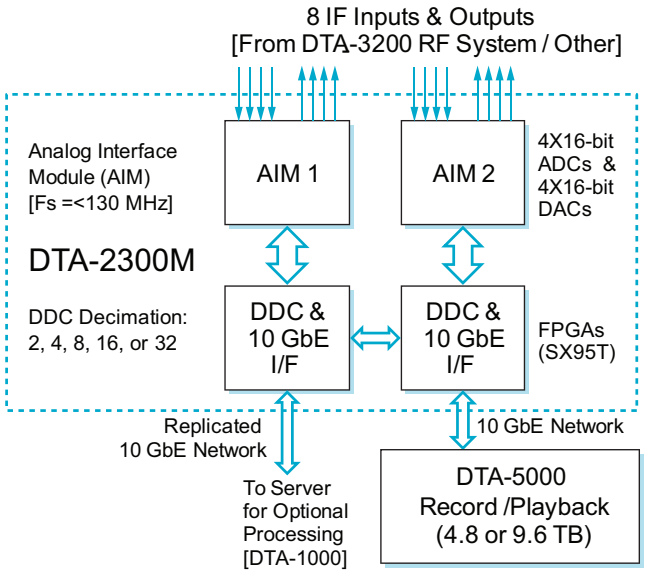
DTA-2300M configuration shown allows real-time recording/playback and processing 20 MHz BW for each of the 16 channels. The M configuration also allows replicated 10 GbE ports for simultaneous recording & processing. For processing bandwidth 10 MHz or less only one DTA-5000 & 1 DTA-1000 may be sufficient for real-time operation

For many HF applications, including phased array radar, SIGINT/COMINT and direction finding, the above configuration offers a complete solution from HF signal conditioning to record/playback and processing. The 3200H system provides up to 16 receive and transmit channels in a 3U enclosure. The DTA-2300M configuration shown here allows simultaneous processing and recording by offering replicated 10 Gigabit networks. For higher than 20 MHz real-time processing bandwidths, the DTA-2300S configuration can be used. For less than 10 MHz processing bandwidths, the Network Interface Card (NIC) inside the server or recorder can combine two 10 GbE data streams.

[Download Tech Note 19 for more information on HF processing]

A LOW-COST, PHASE-COHERENT RECORD AND PLAYBACK SYSTEM FOR UP TO EIGHT WIDEBAND RADIO SIGNALS

A Low-Cost System for Phase-Coherent Record & Playback of Up to 8 Wideband Signals



The Record /Playback System in a rugged portable case with wheels and shock-mounted rack.

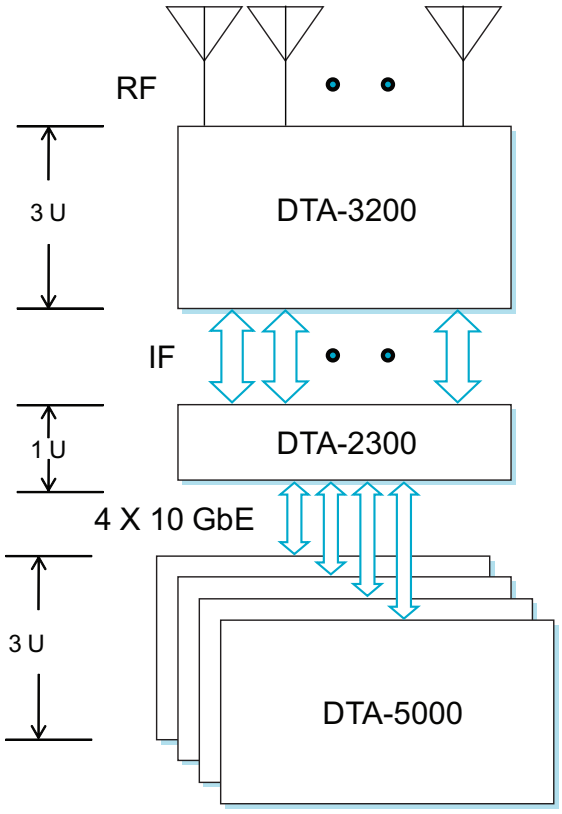
The DTA-2300M configuration provides replicated 10 Gigabit Networks for data, allowing processing using a server while recording. The sustained record/playback rate is 800 MBytes/s. Thus for four IFs, the DDC output rate (Fs/decimation) for each IF can be 100 MHz (the corresponding BW is 40 MHz); for eight IFs, the output rate is 50 MHz for each IF (the corresponding BW is 20 MHz).

The processing bandwidth or the channel count can be increased by doubling the DTA-2300 configuration to 16 channels and using two 10 GbE fibers and two DTA-5000 systems.

The DTA-2300M standard configuration for eight IFs offers 16-bit ADCs and DACs and sample rates up to 130 MHz/channel. A DDC (Digital Down Converter) with programmable decimation (from 2 to 32) for each ADC channel allows programmable selection of bandwidth. The output of the DDC is complex (I & Q) baseband data. The DDC can also be bypassed to store real data. The output data can be real or up-converted to a complex IF signal using the DUC (Digital Up Converter) built in the DACs.

[Download Tech Note TN-18 for more information on this configuration]

A COMPLETE MULTI-ANTENNA SOFTWARE RADIO TRANSCEIVER



RF /IF System
- 20 MHz – 6 GHz Freq. Coverage
- 8 Rx & 8 Tx or 16 Rx/Tx Channels
- 40 MHz BW & 75 MHz IF

IF/Baseband System
- 16 Rx & 16 Tx Channels
- 16 Bit ADCs & DACs, 130 MSPS
- DDC, DUC & 4X10 GbE Networks

Record / Playback
- 800 MBytes/s per 10 GbE Fiber
- 9.6 Terabyte Storage per DTA5000
- Comprehensive GUI

From RF/IF to Record/Playback, D-TA products provide complete software radio solutions for multi-antenna applications that require fully synchronized phase-coherent operations. The DTA-3200 provides a wide frequency coverage and a tunable instantaneous bandwidth of 40 MHz. The DTA-2300 provides 16-bit digitization and DDC for each IF input. It also offers 16-bit DACs and DUCs for IF signal generation for RF up-conversion. The DTA-5000 offers a record/playback rate of over 800 MBytes/s per 10 Gigabit fiber. By using all four fibers and four DTA-5000 units, RF signals from 16 antennas with instantaneous BW of 40 MHz can be recorded or played back in real time.

ARBITRARY WAVEFORM GENERATION

The above configuration can also be used for generating multiple phase-coherent arbitrary waveforms simulation, scenario generation or RF test. Computer-generated data can be recorded in DTA-5000 system(s) for playback through the DTA-2300 and DTA-3200 units.

[Download Tech Note TN-21 for more information on arbitrary waveform generation]

DTA-4100

HIGH CHANNEL-COUNT SONAR/ACOUSTIC SYSTEM

DTA-4100 is designed for high-frequency, high-precision and high-channel-count sonar and acoustic applications. The DTA-4100 is conduction-cooled and connects to the external world via two optical fibers: a 10 Gigabit fiber for data and a 1 Gigabit fiber for control. The DTA-4100, therefore, can be placed close to the sensors. For many complex sonar/acoustics applications, this simplifies cabling issues and avoids having to run analog cables from the sensors over long distances.

DTA-4100 is partitioned into receive (DTA-4100R) and transmit (DTA-4100T) sections. Each section is a conduction-cooled 36-channel system that uses a 10 Gigabit optical network for data and a separate 1 Gigabit optical network for control. DC power (28V) is supplied from an external source. Multiple DTA-4100 Receive and Transmit units can be operated synchronously to handle large sensor arrays. Also, for lower-speed applications, the data from multiple DTA-4100 units can be merged onto one 10 Gigabit network. DTA-4100 is also available in a 19" rack-mountable enclosure configured for user requirements.

DTA-4100 readily plugs into D-TA's 10 Gigabit Sensor Processing infrastructure, which includes real-time processing and record and playback.

[Download Tech Note TN-22 for more information on DTA-4100]

DTA-4100R/T (8.25"(W)X18.25"(L)X1.6"(H))

AT A GLANCE

- Conduction-Cooled Receive & Transmit Systems

DTA-4100R RECEIVE SYSTEM:

- 36 Differential Inputs
- Signal Conditioning with Programmable Gain
- 24-Bit, 2.5 MHz Sigma-Delta ADCs
- Over 100 dB SNR
- Large Virtex 5 FPGA for DSP
- 10 Gigabit Optical Network for Data
- 1 Gigabit optical Network for control
- Multiple DTA-4100R Units can be Operated Synchronously

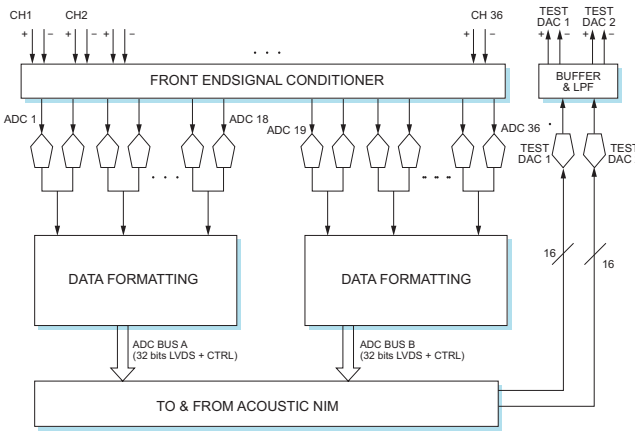
DTA-4100T TRANSMIT SYSTEMS

- 36 Differential Outputs
- 16-Bit, 50 MHz DAC (reconstruction Filter Cut-off 1 MHz)
- Over 80 dB SNR
- Large Virtex 5 FPGA for DSP
- 10 Gigabit Optical Network for Data
- 1 Gigabit optical Network for control
- Multiple DTA-4100T Units can be Operated Synchronously

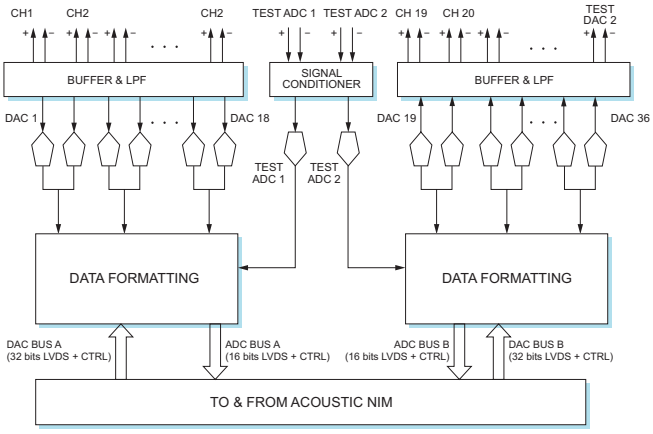
APPLICATIONS

- High-Frequency Sonar / Acoustics
- Mine Sonar, Dipping sonar, Obstacle Avoidance Sonar, ASW Sonar, etc.
- Oversampling beamforming
- Non-Destructive Test
- Sonar / Acoustic Stimulator

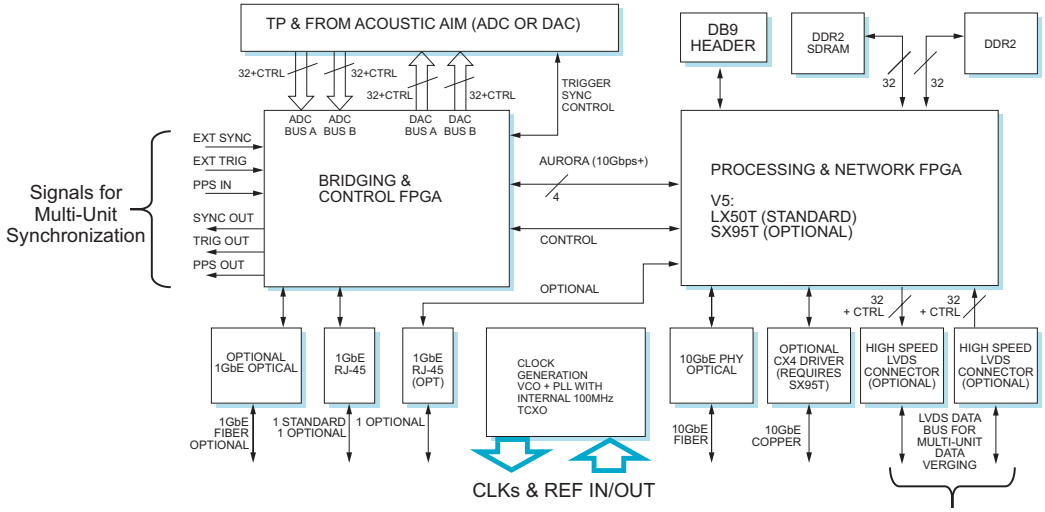
Analog Interface Module (AIM) Receive



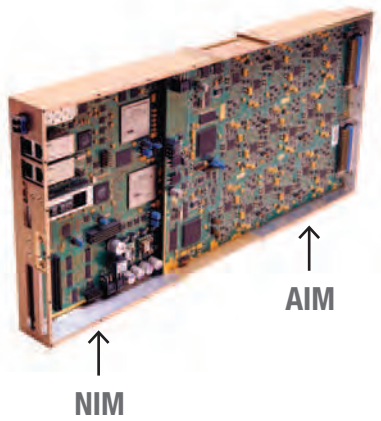
Analog Interface Module (AIM) Transmit

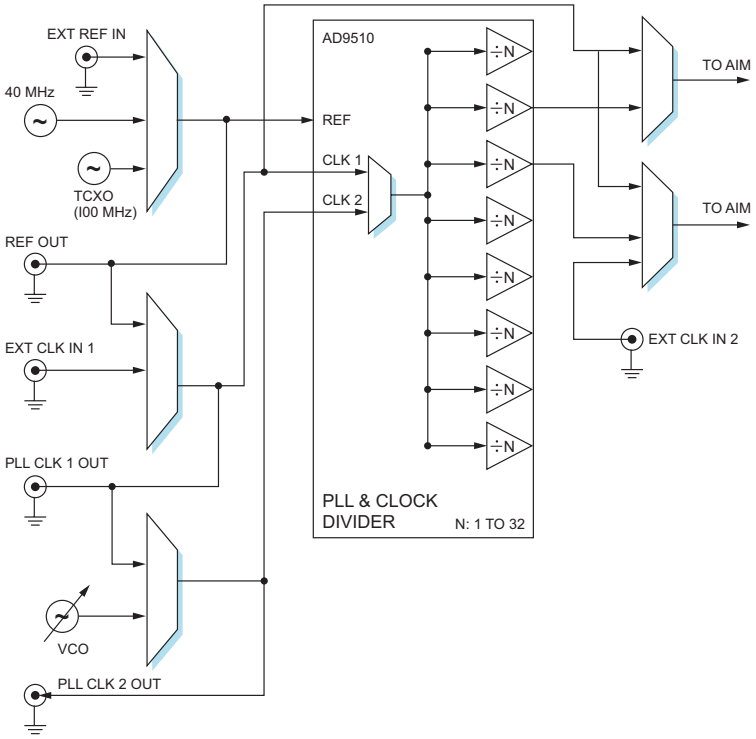


Network Interface Module (NIM)



The DTA-4100 is also available in a 19" rack-mountable enclosure that is configured for the user channel-count and physical requirements





The DTA-4100 provides flexible clocking options. The ADC and DAC clocks can be supplied externally or generated by dividing down a stable 100 MHz internal TCXO. They can also be generated by a VCO locked to an external reference. For synchronizing multiple DTA-4100 units, the ADC and DAC clocks are generated in one DTA-4100 designated as master and are transmitted to all slave units.

DTA-4100 is also available in a 19" rack-mountable enclosure that is configured for the user's channel-count and physical requirements.

Both Receive and Transmit AIMs are identical in structure. The receive AIM includes two DACs while the transmit AIM includes two ADCs. The NIM includes two FPGAs. The control FPGA connects to the AIM and transfers data to the processing FPGA (user programmable) that also holds the 10 Gigabit network core. The NIM also includes two banks of DDR2 memories (128 Mbytes) and a header for digital I/O. The AIM and NIM are both conduction-cooled modules that are housed in a 18.25"(L) X 8.25"(W) X 1.6"(H) enclosure with heat pipes for heat conduction through the surface. DTA-4100 R/T units are also offered in a 19" rack-mountable enclosure.

The Receive (ADC) AIM includes 36 differential input channels divided into two equal halves. The front-end signal conditioning includes programmable gain up to 42 dB and 4-pole anti-alias filtering. The default low-pass filter cutoff frequency is 1 MHz. It can also be factory set to meet user requirements. The ADCs are 24-Bit Sigma-Delta ADCs (Analog Devices AD7760) that provide an effective sample rate (output rate) of up to 2.5 MHz/channel. The ADC AIM module also includes two differential DAC output channels for test. For many sonar applications where all transducers are excited by the same waveform (e.g., OMNI transmit), the DTA-4100R can be used for both receive and transmit.

The Transmit AIM includes 36 differential output channels that are also divided into two equal halves. The output signal conditioning for each channel includes 4-pole reconstruction filtering with a cutoff frequency of 1 MHz and high-current drive differential output amplifiers. The DACs are 16-bit 50 MHz DACs; therefore, they can be operated at a higher-than-required rate for good image rejection. The reconstruction filters can be customized to user requirements. Like the ADC AIM, the DAC AIM includes two differential input channels for test.

MAJOR SPECIFICATIONS

ITEM	DTA-4100R (RECEIVE)	DTA-4100T(TRANSMIT)	COMMENTS
No. of Channels	36 Differential	36 Differential	
Impedance	10K Ohm	50 Ohm	
Gain	40 dB Programmable		
Data Converter Resolution	24 Bits	16 Bits	
Max. Data Conversion Rate	2.5 MHz (ADC output rate)	50 MHz	
Filter Characteristics	4-Pole Low Pass with 1 MHz Cutoff Frequency	4-Pole Low Pass with 1 MHz Cutoff Frequency	Can be customized
SNR	105 dB	80 dB	
FPGA	Xilinx Virtex 5, (SX95T)	Xilinx Virtex 5, (SX95T)	User access is allowed for DSP core development
Data Network	10 Gigabit Optical (UDP)	10 Gigabit Optical (UDP)	
Control Network	1 Gigabit Optical (UDP)	1 Gigabit Optical (UDP)	
Power	28 V DC, 5 Amps	28 V DC, 5 Amps	
Operating Temp	-10° C – +50° C	-10° C – +50°0 C	
Size			

[Specifications may change without notice]

LEVERAGING 10 GIGABIT SENSOR PROCESSING INFRASTRUCTURE

The 10 Gigabit sensor processing infrastructure developed by D-TA for the Radio products is readily adaptable for sonar/acoustic sensor processing. Scalable Record/Playback and Multi-Core server processing are two key benefits of standardization on the 10 Gigabit Sensor Processing architecture. D-TA's DTA-5000 RAID based record/playback offers up to 9.6 Terabytes of storage capacity and a record/playback rate of over 800 MBytes/s per DTA-5000 units. This means that 144 channels @1.85 MHz/ch sample rate (24-bit data) can be recorded in real time using only one DTA-5000 system. For most sonar/acoustic applications, however, the data rate is much lower and a lot more channels can be recorded and played back using just one 10 Gigabit network.

[Download Tech Notes 11, 18 and 25 for more information on record/playback]

For post-processing, the low-cost DTA-1000 server (a commercially available 8-core server) system provides significant processing capability. The DTA-1000 server system is pre-installed with a 10 Gigabit NIC card and D-TA SDK (Software Development Kit). The D-TA SDK helps users develop multi-threaded software for Multi-Core processing. D-TA also offers application development support and training.

[Download Tech Note 14 for more information on D-TA's software architecture]

SONAR/ACOUSTIC SIM/STIM

Sonar/Acoustic Sim/Stim (Simulation/Stimulation) is used for test, scenario generation and training. Real-time generation of multi-sensor acoustic signals is easily accomplished by using the DTA-5000 storage system in the playback mode to drive DTA-4100T units(s) via the 10 Gigabit network. DTA-5000 can hold as much as 9.6 Terabytes of data to enable long-term scenario generation. Either pre-recorded data or computer-generated data can be played back. Data generated in a computer is transferred to DTA-5000 via the 1 GbE network. For user convenience, DTA provides software to facilitate conversion of user-generated data files (using MATLAB or other programs) into data formats accepted by DTA-5000.

OVERSAMPLING BEAMFORMING

DTA-4100 offers high sampling rates (up to 2.5 MHz) and high precision (24-bit). Most sonar systems require much lower sampling rates because of their typically low bandwidth requirements. The high-sampling-rate capability of DTA-4100 system can be exploited to provide oversampled signals for convenient beamforming in the computer (or in the onboard FPGA). The availability of the 10 Gigabit data link(s) means that there is little or no data bandwidth restriction for high-speed data transfer to the computer (like with the DTA-1000).

The oversampling beamforming requires no computation, other than shading (windowing) of channel data and adding up the appropriate samples of each channel. The shading operation can be done by the FPGA onboard DTA-4100. Thus, the only arithmetic operation required is the addition of channel samples (pre-shaded) for each beam. Real-time operation, therefore, is easily achievable.

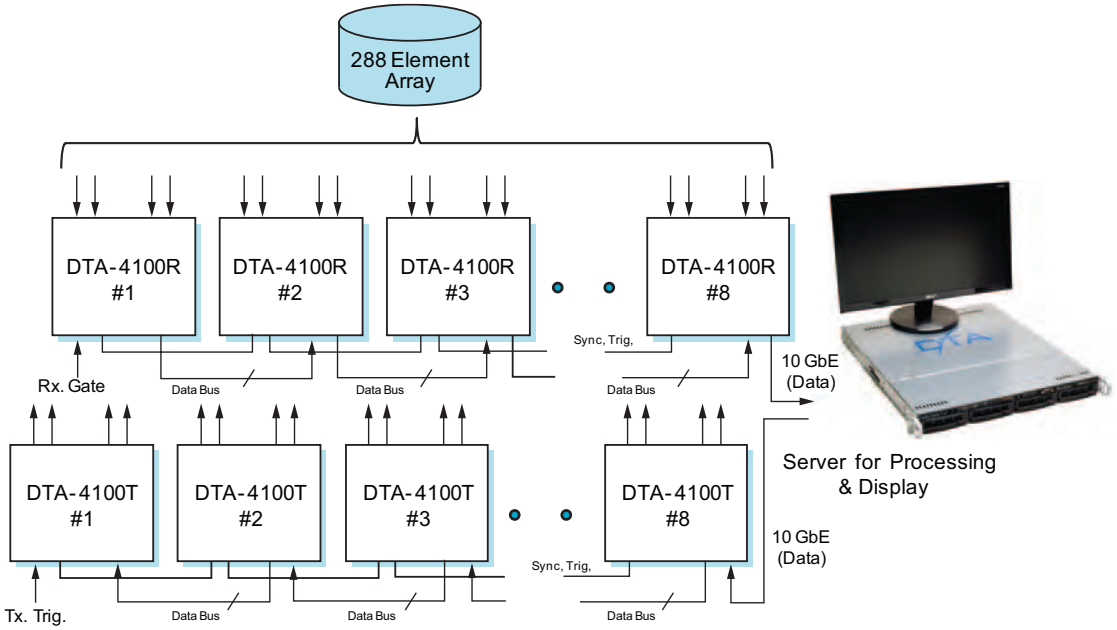
The oversampling beamforming approach not only offers significant computational savings, but is also more accurate than conventional interpolation beamforming. Using interpolation to simulate oversampling suffers from errors due to finite length FIR interpolation filtering. The DTA-4100's high-speed 24-bit ADCs offer more accurate sampling than is practical to simulate by interpolation filtering.

[Download Tech Note TN-23 for more information on oversampling beamforming]

ORDERING INFORMATION

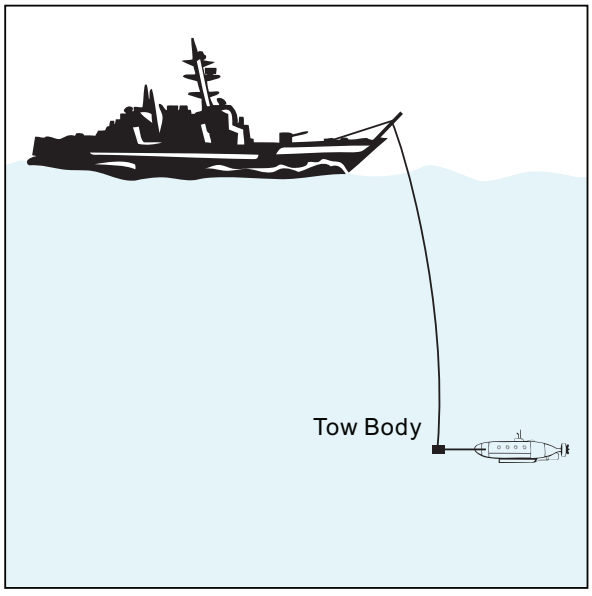
PART NO.	DESCRIPTION	REMARKS
DTA-4100C-xR	Conduction-cooled Receive Module (x=no. of channels=8, 16, or 36) with a 10 Gigabit network	
DTA-4100C-xT	Conduction-cooled Transmit Module (x=no. of channels=8, 16, or 36) with a 10 Gigabit network	
DTA-4100S-xRT	19" Rackmountable Receive/ Transmit System with (x=channel count) 10 Gigabit Network(s)	
SDK-4100	Software Development Kit	
FDK-4100	Firmware Development Kit	
DTA-1000-R	1U Dual Quad-Core Server with 8 TB storage and with 10 GbE NIC and SDK Pre-installed	Also available without storage

DEPLOYING DTA-4100 FOR ASW, MINE AND DIPPING SONAR APPLICATIONS

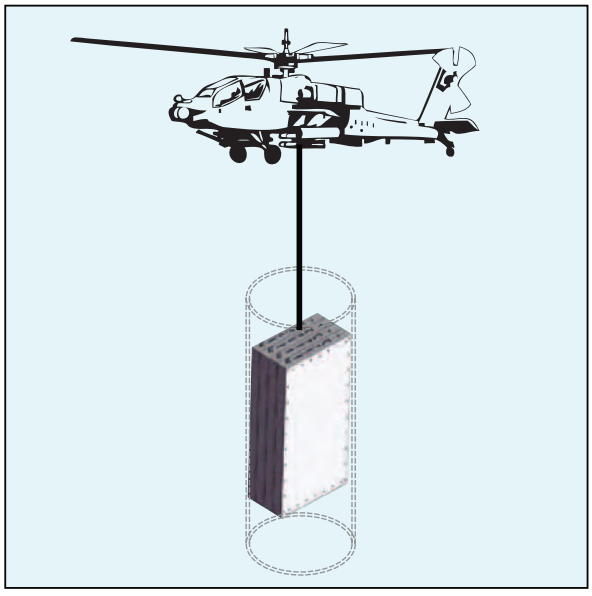


In ASW sonar applications, the multiple DTA-4100s can be stacked to meet the channel count requirement. Typically, low sample rates mean that data multiple DTA-4100s can be merged onto one or two 10 GbE fibers. The cabling issues are significantly simplified by placing the DTA-4100s close to the sensors.

DTA-4100 is particularly well suited for Dipping sonar and Mine sonar that deploy a tow body.



Fibers carry data from the ship to the tow body that includes the DTA-4100(s).



Up to four DTA-4100s can be included in an 8" diameter tube close to the sensors. Optical fibers connect the DTA-4100s to the processor onboard the aircraft.

DTA-9500

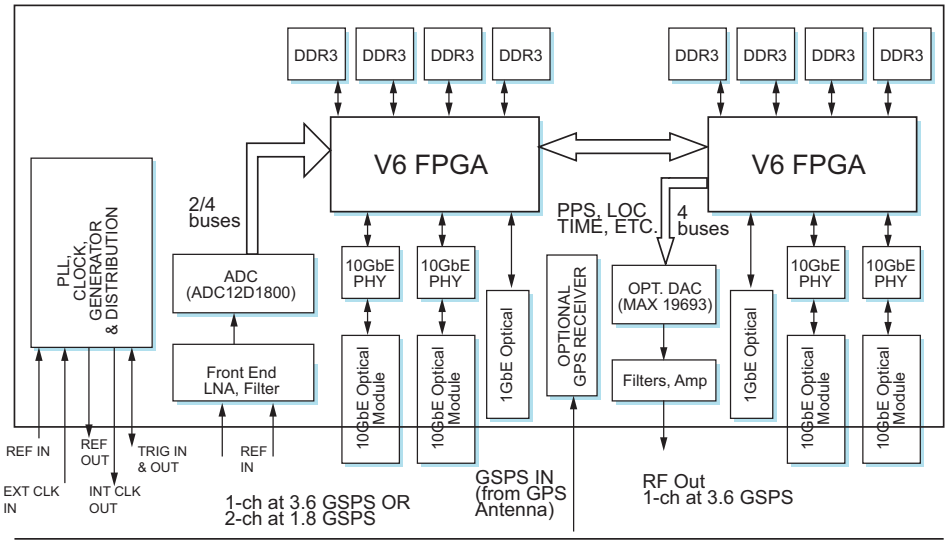
CONDUCTION-COOLED ULTRA WIDEBAND RECEIVE & TRANSMIT SYSTEM

AT A GLANCE

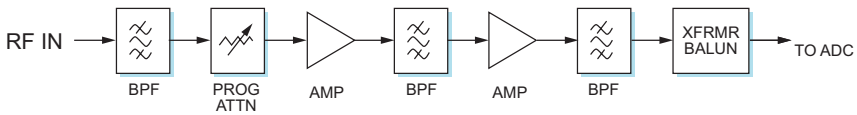
- 12-Bit ADCs Provide 2 Channels @1.8 GSPS or 1 Channel @ 3.6 GSPS
- RF Front End with Programmable Gain & Filter (Customizable)
- Two Virtex 6 FPGAs (V6 – LX130T Upgradable to SX315T) for Processing (User Programmable)
- Digital I/Os Connected to FPGA
- 1GBytes of DDR3 SDRAM (4 Banks per FPGA)
- Flexible Clocking Options (Internal, External Ref., GPS etc.)
- Four 10 Gigabit Optical Network for Real Time Data Recording with DTA-5000s at Full Speed or Processing with DTA-1000 Servers.
- Separate 1 Gigabit Optical Network for Control
- Optional GPS Receiver
- Optional 4 GHz DAC Output
- Multi-Unit Synchronization
- Conduction-cooled 11" (W)X11"(L) X 3.5" (H)
- 28 V @ 18 A Power Input

APPLICATIONS

- Radio Head
- Radar ELINT
- COMINT /SIGINT
- Wideband Communications
- High-Energy Physics
- Arbitrary Waveform Generation



DTA-9500 Block Diagram



DTA-9500 RF Front End
(Filters can be user specified)

DTA-6800

CONDUCTION-COOLED VIRTEX 6 BASED FPGA PROCESSING FARM

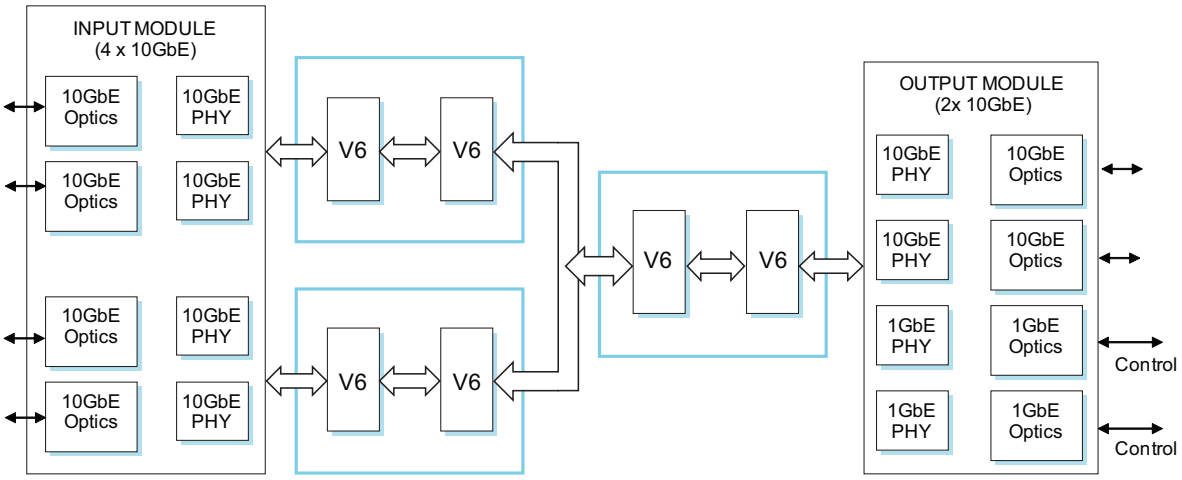
AT A GLANCE

- Up To Six (6) Virex 6 FPGAs (User Programmable)
- Up To 3 Gigabytes DDR3 SDRAM (four banks per FPGA)
- Up To Six (6) 10 Gigabit (GbE) Optical Networks
- Separate 1 Gigabit Optical Network for Control
- Can be configured for Direct Interfacing to All D-TA 10 GbE Network Attached Products
- Firmware Development Kit & factory support for user FPGA Core Development
- Multi-Unit Synchronization
- Conduction-cooled Enclosure
- 28 V @ 25A Power Input

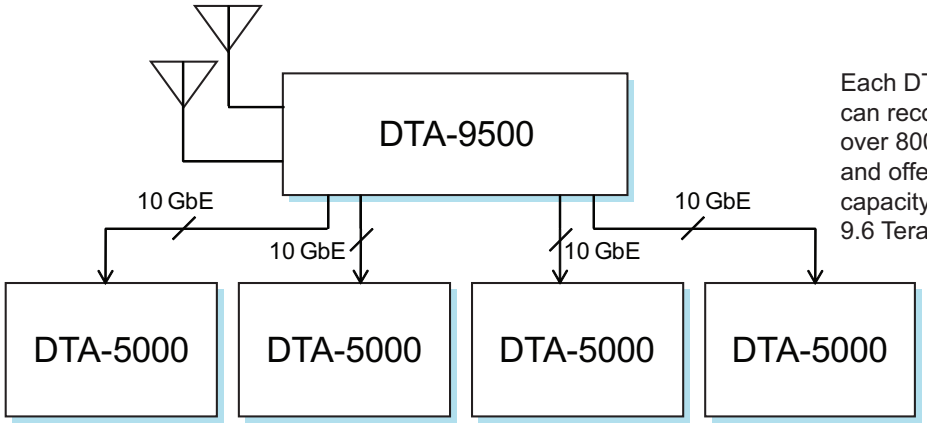
APPLICATIONS

- High Volume FPGA Processing
- Add FPGA Processing Power to DTA-9500, DTA-2300, DTA-4100 & DTA-5000 Systems
- Configurable 10 GbE Switch

DTA-6800 Block diagram



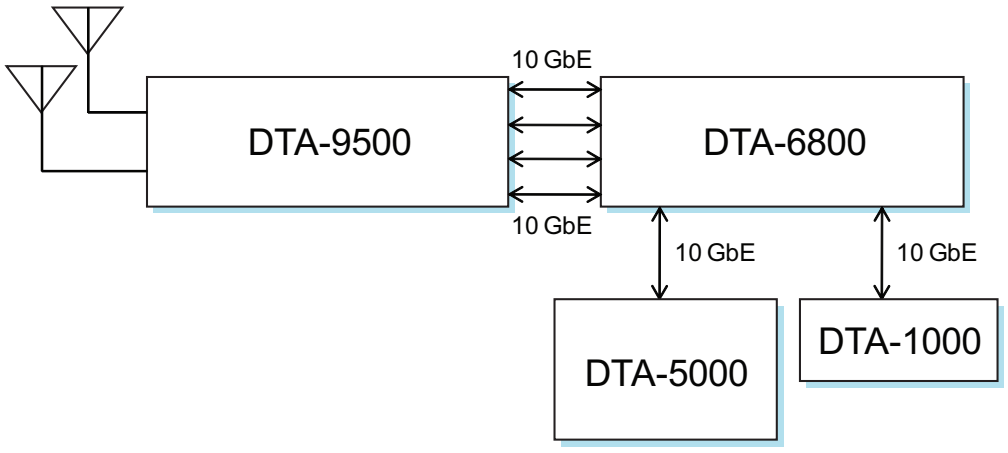
SUSTAINED RECORDING AT 3.2 GSPS RATE WITH DTA-9500



Continuous recording of ADC data sampled at up to 3.2 GHz for one channel or 1.6 GHz for two channels. Four DTA-5000 systems (each running at a sustained rate of 800 MBytes/s) are used in a time-multiplexed fashion (samples 1, 5, 9...in one recorder; samples 2, 6, 10...in another one, and so on). Synchronous operation maintains time integrity of samples and convenient reconstruction of ADC data for analysis. For this operation, 12-bit ADC data is rounded to 8 bits by the FPGA(s) to meet the maximum recording rate constraint.

The use of optical networks allows the DTA-9500 to be placed far away (close to the antennas, if required) from the recorders.

REAL-TIME FPGA PROCESSING OF MULTI-GHz BW RADIO SIGNALS



The use of DTA-6800 adds significant processing power (a total of up to eight Virtex 6 FPGAs) for wideband communications and radar applications. The DTA-6800 can be configured for four 10 GbE inputs for accepting ADC data at the full sampling rate, and two 10 GbE outputs for processed data. The figure shows replicated 10 GbE output networks for simultaneous recording and processing.

Software and Firmware Development

SOFTWARE DEVELOPMENT KIT AND APPLICATION DEVELOPMENT

All D-TA products have an associated C++ Software Development Kit (SDK) that provides the framework for real-time application development in a Multi-Core server environment. The SDK has three parts: Control SDK, Data SDK and Optional Real Time DSP Modules. The SDK is written in POSIX-compliant C++ code (full source code available) for Linux. The SDK abstracts all socket calls and speeds up application development. Example codes are included with the SDK to ease integration and provide an "out of the box" experience.

Control SDK: contains all the APIs required to control the D-TA products. The API is organized into functional modules that abstract the need for users to understand the register structure of the device in details. Alternatively, for more advanced users, a set of Atomic API functions allows direct read/write access to all the registers. The code structure is modular, and the user can always add specific user control functions to customize the SDK.

Data SDK: is designed for receiving and transmitting 10 GbE data to and from the DTA product. It is architected in a manner to make it similar across all the D-TA products The Data SDK allows abstraction of data transfer to and from the D-TA products and enables the user to concentrate on application development.

Real Time DSP Modules: are easily created from template classes provided. The creation of these modules has been simplified so that the user need specify only a few parameters, such as the CPU cores to run on, number of threads to handle the data, and thread affinity. After specifying these parameters, the user only has to implement an algorithm. The module is compiled into its own dynamic library that can be loaded at run time from the user data project.

DTA-1000: An Integrated Server for Developing Real-Time Processing Modules

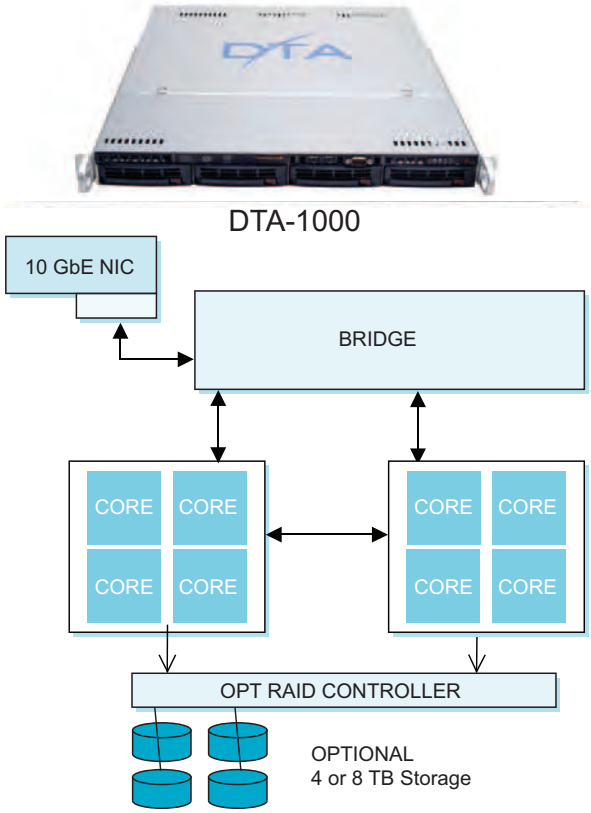
The DTA-1000 is an integrated solution that includes a high-performance server (Supermicro quad core dual Xeon machine) integrated with the NIC, together with all system software tuning required for best performance. The system includes:

- **Dual Xeon (quad core) server class of machine**
- **Linux OS (kernel 2.6.26) with real-time patch**
- **Kernel tuning for highest performance with DTA-2300**

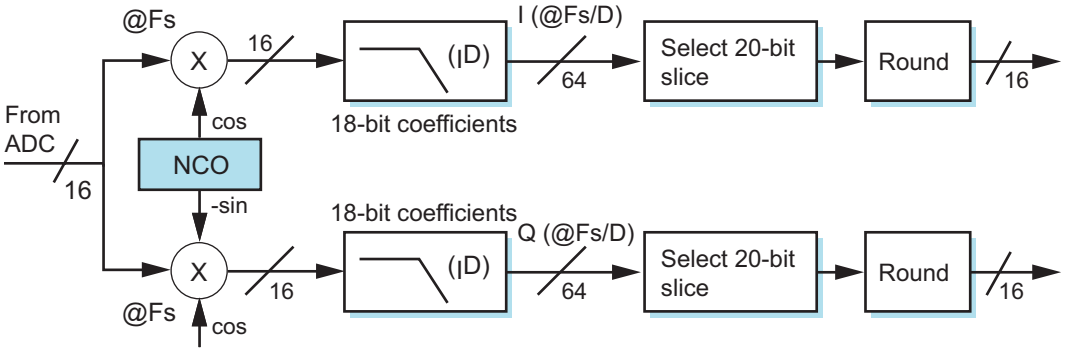
This allows another level of system integration that allows rapid prototyping and deployment. The appropriate SDK is pre-installed and all example codes are ready to run. The DTA-1000 is an extremely cost-effective method of rapid prototyping and quick deployment.

The DTA-1000 can be optionally configured with up to 8 TB of storage.

We also offer application development support for quick deployment using our expertise in multi-threaded, Multi-Core software development expertise. Our expertise and the Software Development Kit (SDK) simplify easy development of real -time processing modules for today's high-performance Multi-Core servers. The SDK allows users to harness the immense and ever-increasing processing power of servers, and to develop applications that are scalable with server performance, thereby keeping ahead Tech Note 14 for more information.



FIRMWARE DEVELOPMENT KIT AND FPGA DEVELOPMENT



D-TA products have an optional Firmware Development Kit that includes the full source code for the user-programmable FPGA in the product (DTA-2300, DTA-2210, DTA-3290, DTA-9500, DTA-6800, DTA-4100, etc.). The FDK is delivered in the Xilinx ISE environment and allows users to modify and add VHDL-based DSP processing modules. Some Xilinx files (e.g., the 10 GbE MAC) are included only as netlist files.

D-TA has off-the-shelf cores – programmable DDC, FFT, WOLA FFT, etc. – that can be easily integrated to expand the capability of the product. The programmable DDC functionality is provided as a standard configuration with DTA-2210, DTA-3290 and DTA-2300. The programmable DDC offers a software-programmable decimation rate of 2, 4, 8, 16 or 32, together with programmable filter coefficients. The DDC implementation is shown below.

The design allows maintains full precision internally to minimize cumulative rounding errors and implements a user-programmable scaling function.

Because we are aware of the fact that FPGA development involves significant specialized effort and may be an expensive proposition for some of our customers, we undertake customized FPGA development for user-specific applications. Please contact us to discuss your requirements and for more information.

Customer Support

WEBSITE RESOURCES

D-TA Systems has published a large number of Technical Notes that provide detailed product descriptions, technical features and application examples. These Technical Notes can be downloaded from our website at www.D-TA.com.

TRAINING

D-TA Systems provide software application development and FPGA core development support for rapid prototyping. The D-TA SDK & FDK (Software & Firmware Development Kits) are designed to help user development by providing design strategies, full source codes and application examples. D-TA Systems also offers custom application development services and hand-on training. The training is offered either at customer location or at D-TA facilities in the USA, Canada or Europe. Contact factory for more information.

VIDEO DEMO

Prospective customers can request a free video demo of any D-TA product. An on-site demo is also offered in special situations. Please contact D-TA sales for details.

FACTORY ACCEPTANCE TEST (FAT)

A customer can request an FAT prior to delivery. The FAT is typically performed at the factory in the presence of a customer representative. The FAT can also be done via video. Please note that the FAT is a cost item.

SHIPPING AND DELIVERY

Our prices are quoted as FOB factory, and the customer is responsible for paying for all, shipping, transportation, and applicable taxes and duties. Please provide us with your FedEx/courier account number if you wish to use your own account. Optional rugged cases are offered for field-deployable solutions.

STANDARD AND EXTENDED WARRANTY

All D-TA products carry a standard warranty of one year from the ship date. During the warranty period, D-TA will repair or replace (solely at D-TA's choice) the product to ensure that it is free of any defects. Standard wear and tear and any damages caused by improper use are excluded from the warranty coverage. For software fixes, D-TA will either email the updated software or make it available for download from an FTP site. For hardware fixes, the customer must ship the product back to the factory. The customer is responsible for shipping charges to ship the product back to the factory. D-TA will ship the repaired (or replaced) product back at its own expense.

An RMA number is required to ship the product back to the factory. Please contact your sales contact to discuss warranty service, or email support@D-TA.com.

EXTENDED WARRANTY

We also offer an optional extended warranty that provides coverage for an additional one or two years. Please contact your sales contact to discuss this option.

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SENSOR PROCESSORS THAT DRASTICALLY REDUCE DEPLOYMENT TIME AND COST

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